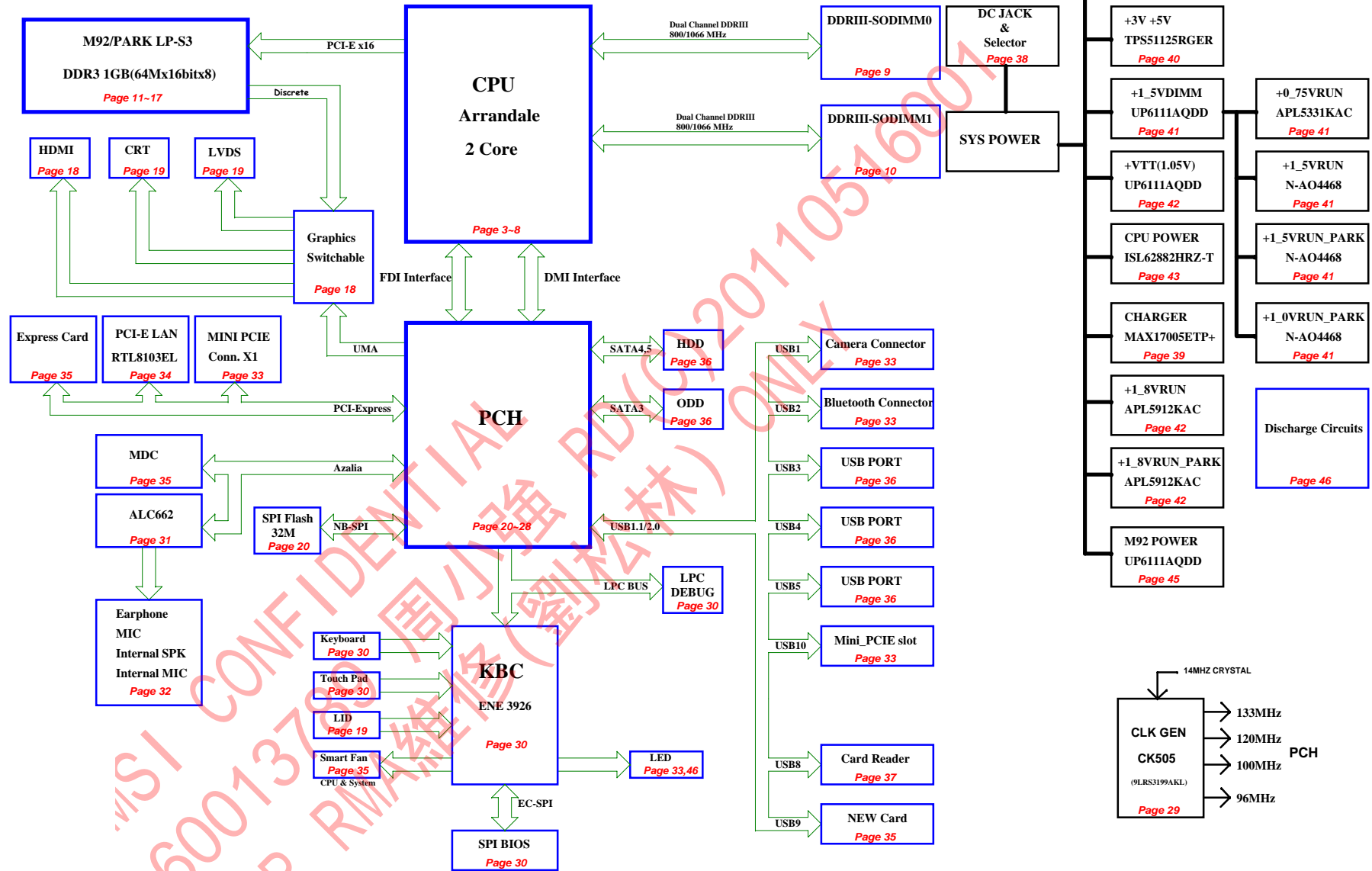


MS-1453(Switchable) & MS-1454(UMA) Ver : 10

2009/07/07

Calpella Platform

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01	BLOCK DIAGRAM
02	PLATFORM
03	PROCESSOR-1 (HOST BUS)
04	PROCESSOR-2 (DDR3)
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07	PROCESSOR-5 (GND)
08	PROCESSOR-6 (RESERVE)
09	DDR3 SODIMM 0
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11	M92/Park-Sx(PCI_E_Interface)
12	M92/Park-Sx(Main_IO)
13	M92/Park-Sx(MEM_Interface)
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16	DDR2(64MX16bit)
17	M92/Park-Sx(Straps&Thermal)
18	SWITCH&HDMI
19	CRT&LVDS
20	PCH-1 (HDA,JTAG,SATA)
21	PCH-2 (PCI-E,SMBUS,CLK)
22	PCH-3 (DMI,FDI,GPIO)
23	PCH-4 (LVDS,DDI)
24	PCH-5 (PCI,USB,NVRAM)
25	PCH-6 (GPIO,VSS_NCTF,RSVD)
26	PCH-7 (POWER)
27	PCH-8 (POWER)
28	PCH-9 (GND)
29	Clock Generator (9LRS3199AKL)
30	KBC/EC/uP (KB3926)
31	CODEC(ALC662)&Amp
32	AUDIO JACKS
33	MINIPICIE,CAMERA,BLUETOOTH,SW
34	PCIE 10/100 LAN (RTL8103EL)
35	NEWCARD,FAN
36	HDD,CDROM,USB
37	Cardreader (RTS5159)
38	M_Battery select
39	M_Battery Charger
40	M_System Power
41	SMDDR_VTERM/1_5VRUN
42	VTT POWER,+1.8VRUN
43	M_CPU power
44	M_Graphic Core
45	M92/Park power
46	Discharge Circuits
47	LED BOARD
48	Screw / EMI
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51	M92/PARK Power on Sequence
52	M92/PARK Power down Sequence
53	Switchable Power Sequence
54	Power MAP
55	Topology
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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

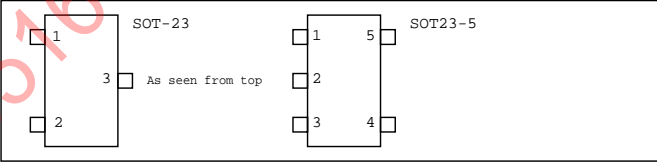
Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
PWR_SRC	19V	S0,(S3-S5)	LAN DDRIII core PCH DDRIII command & control pull up. CPU core rail Graphics core rail (Dual Core only)
+5VALW	5V	S0,(S3-S5)	
+5VRUN	5V	S0	
+5VSUS	5V	S0	
+3VALW	3.3V	S0,(S3-S5)	
+3VSUS	3.3V	S0,(S3-S5)	
+3VRUN	3.3V	S0	
+1_5VDIMM	1.5V	S0,S3	
+1_5VRUN	1.5V	S0,S3	
VTT	1.05V	S0	
+0_75VRUN	0.75V	S0	
+VCC_CORE	1.05V-1.1V	S0	
+VCC_GFXCORE	1.1V	S0	
M92S_VDD_CORE	0.95V	S0	
+1_8VRUN_PARK	1.8V	S0	
+1_5VRUN_PARK	1.5V	S0	
+1_0VRUN_PARK	1.0V	S0	
VDDR3	3.3V	S0	

Net Naming Conventions

Suffix
= Active Low Signal
Prefix
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

PCB Footprints



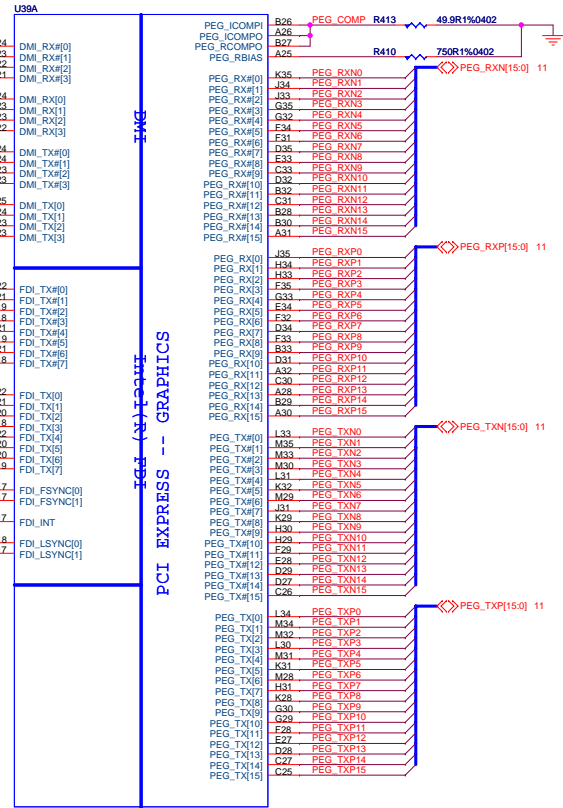
AC Mode

Power States	SLP_S3#	SLP_S4#	SLP_S5#	SLP_LAN#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF

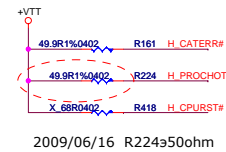
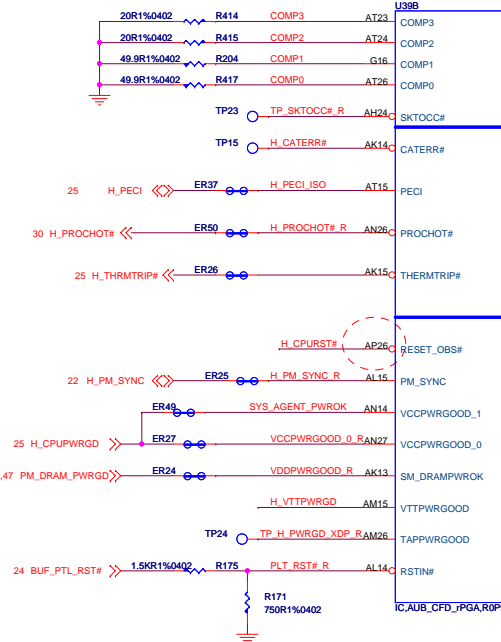
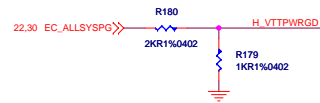
Battery Mode

Power States	SLP_S3#	SLP_S4#	SLP_S5#	SLP_LAN#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	OFF	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF

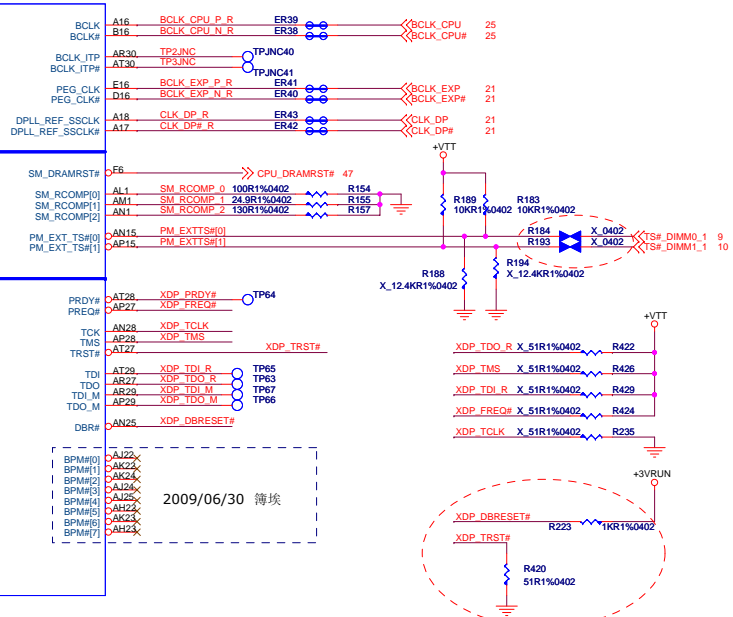
ARRANDALE PROCESSOR (CLK,MISC,JTAG)



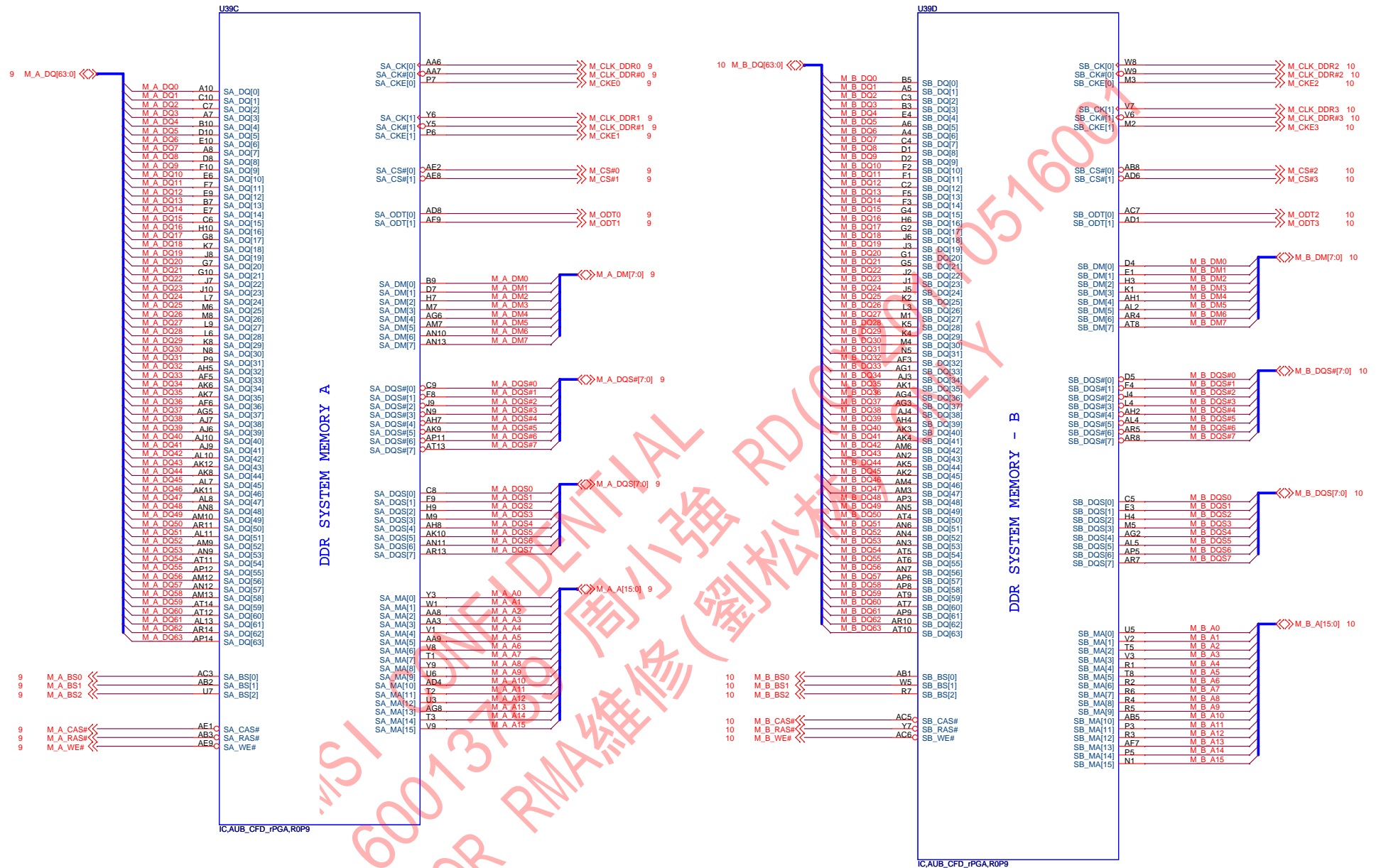
N12-988010-L06
 PGA989
 IC:AUB_CFD_PGA.R0P9



2009/06/16 R224±50ohm



ARRANDALE PROCESSOR (DDR3)

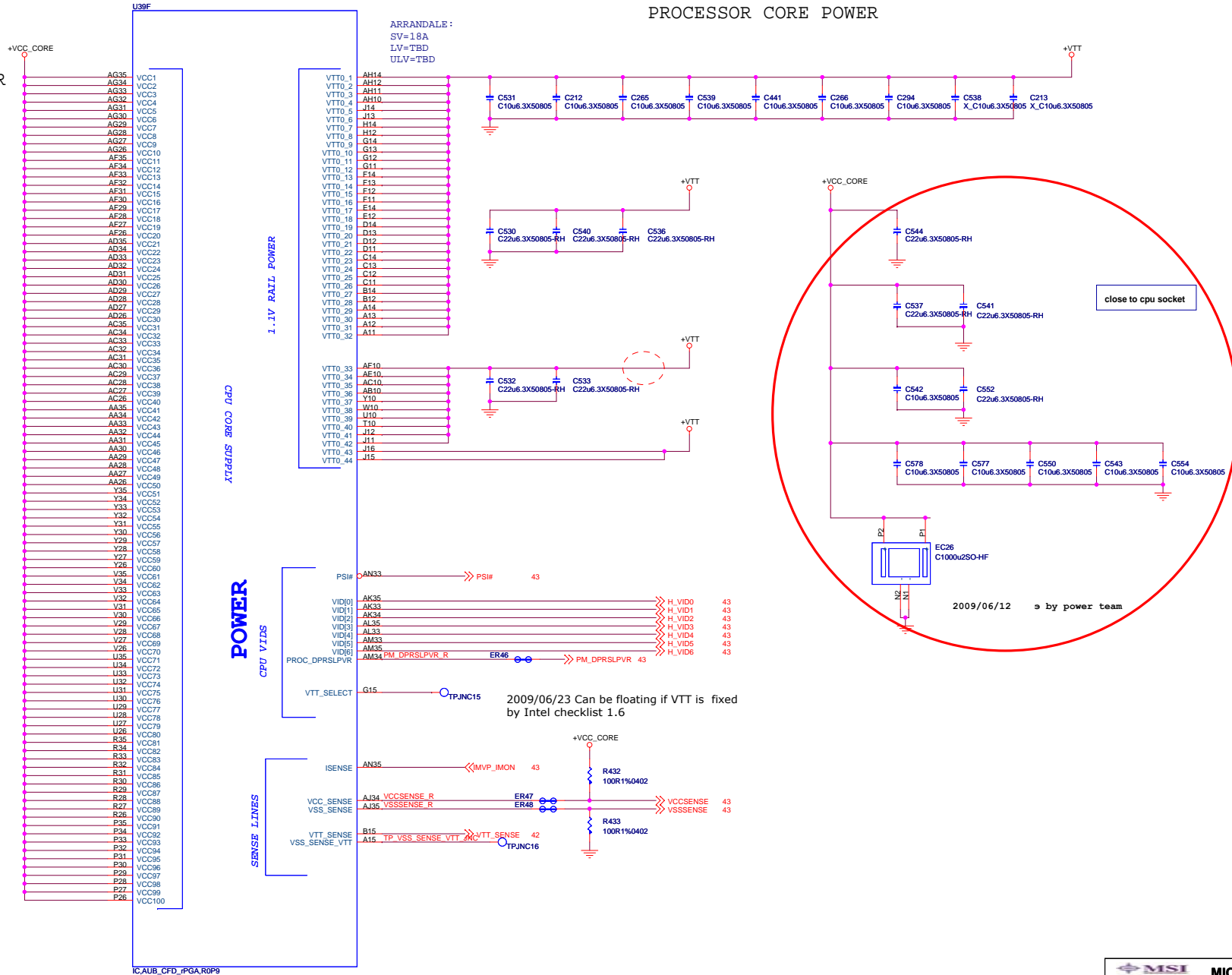


ARRANDALE PROCESSOR (POWER)

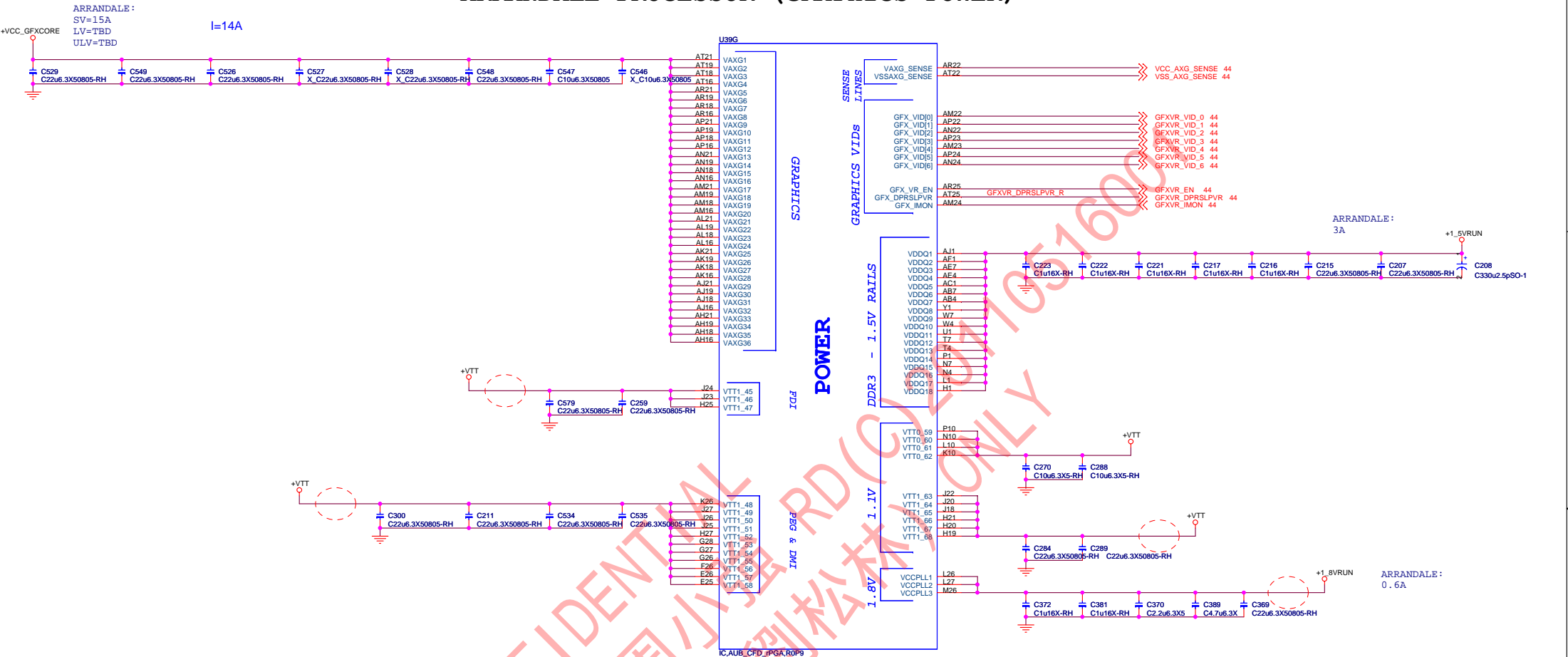
ARRANDALE:
SV=48A
LV=35A
ULV=27A

PROCESSOR CORE POWER

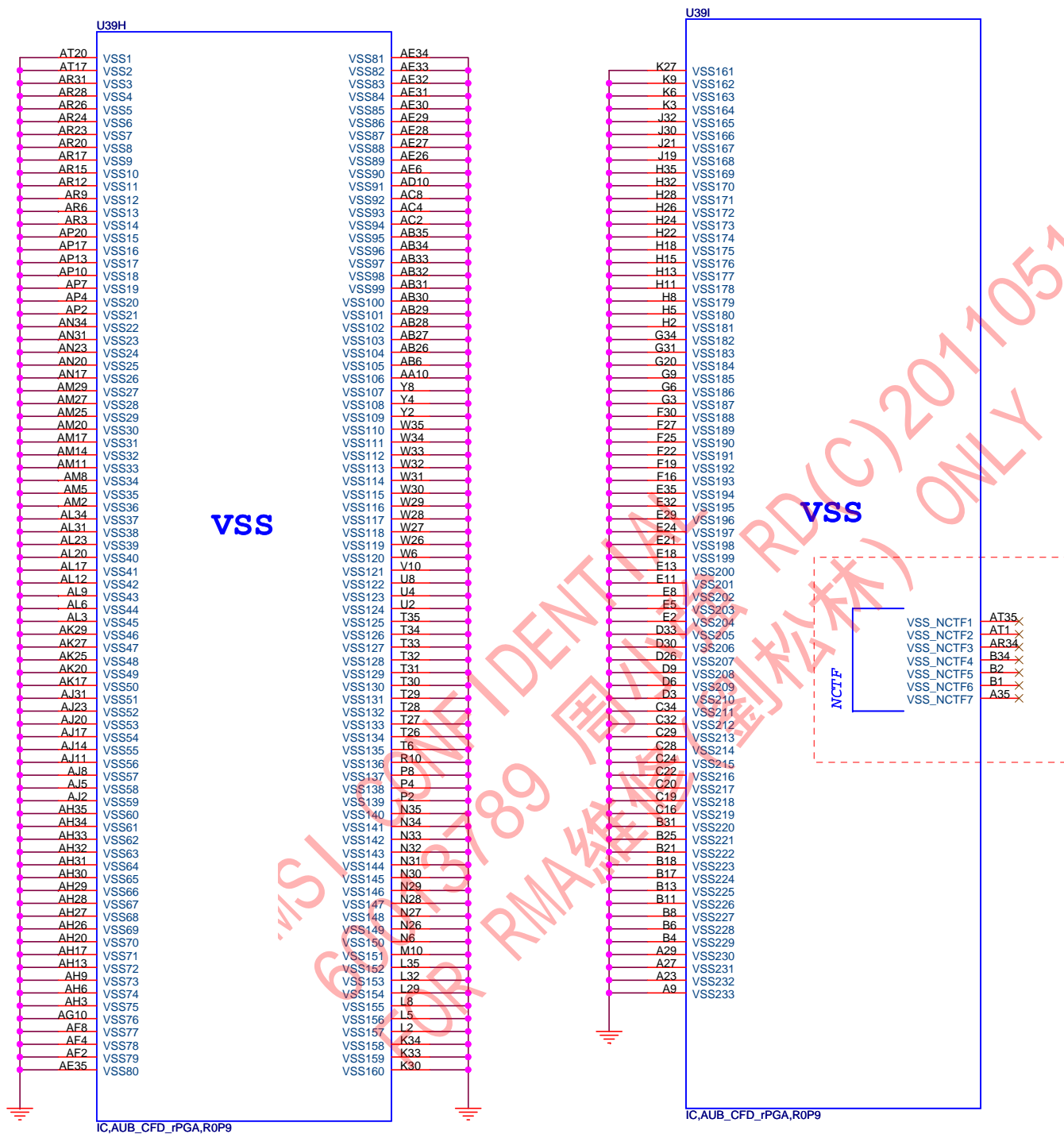
PROCESSOR CORE POWER



ARRANDALE PROCESSOR (GRAPHICS POWER)

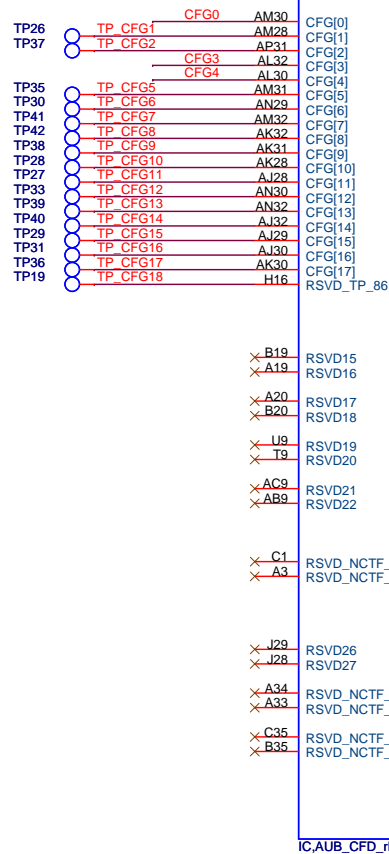


ARRANDALE PROCESSOR (GND)

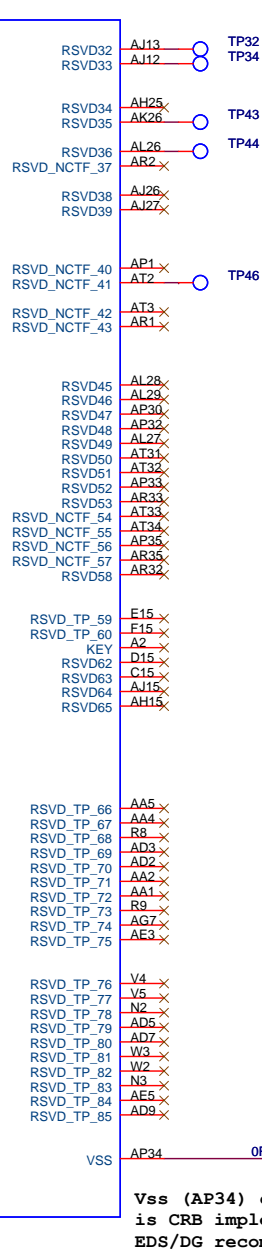


ARRANDALE PROCESSOR (RESERVED)

2009/06/30 Only reserved CFG TP

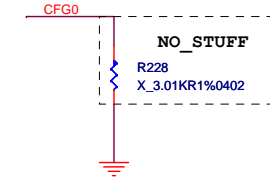


RESERVED

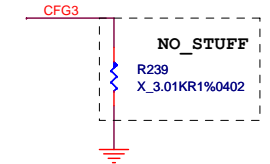


Vss (AP34) can be left NC
is CRB implementation;
EDS/DG recommendation to GND

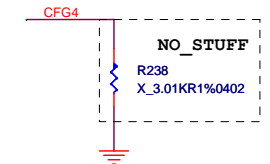
PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled



CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

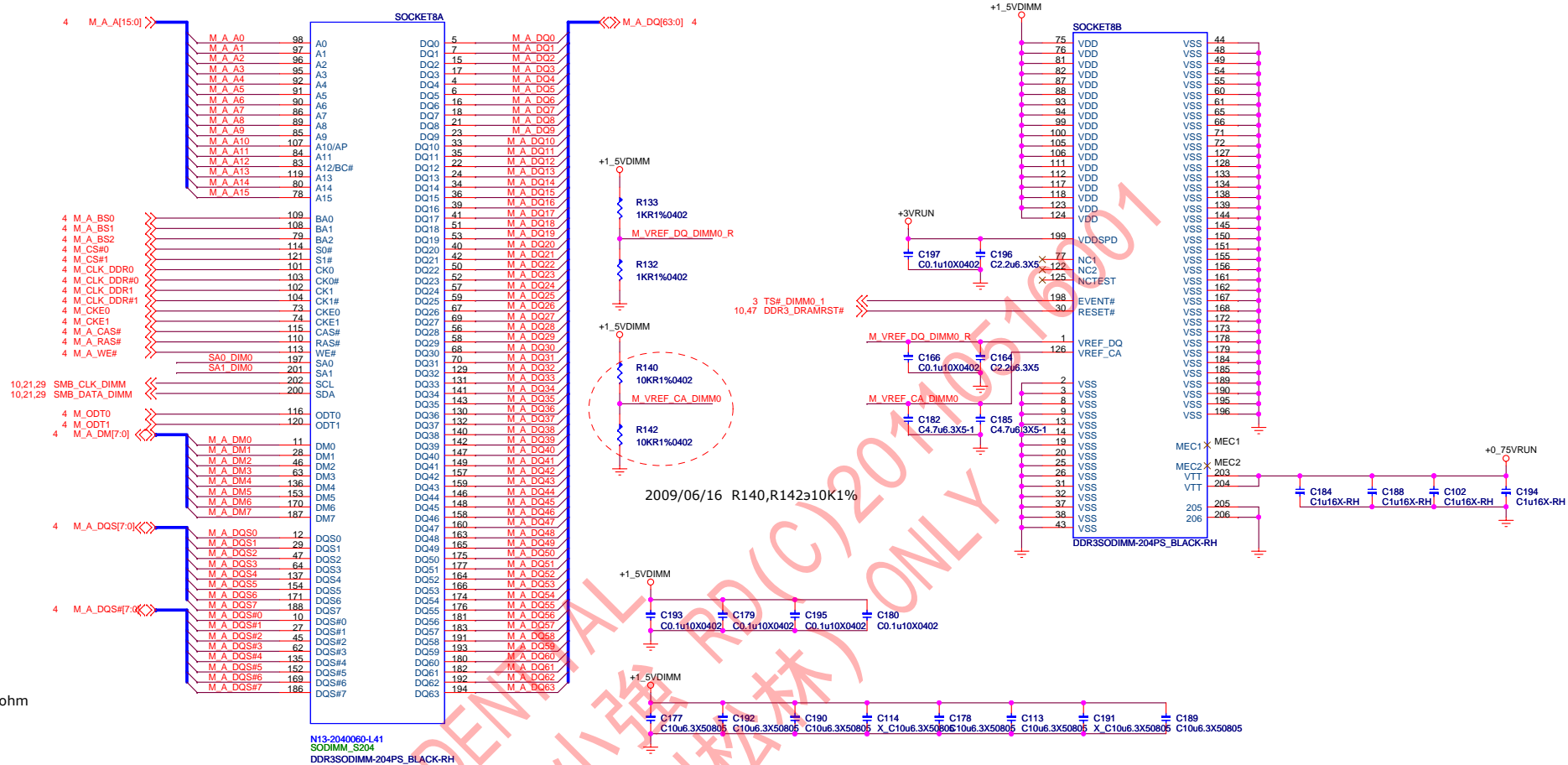


CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

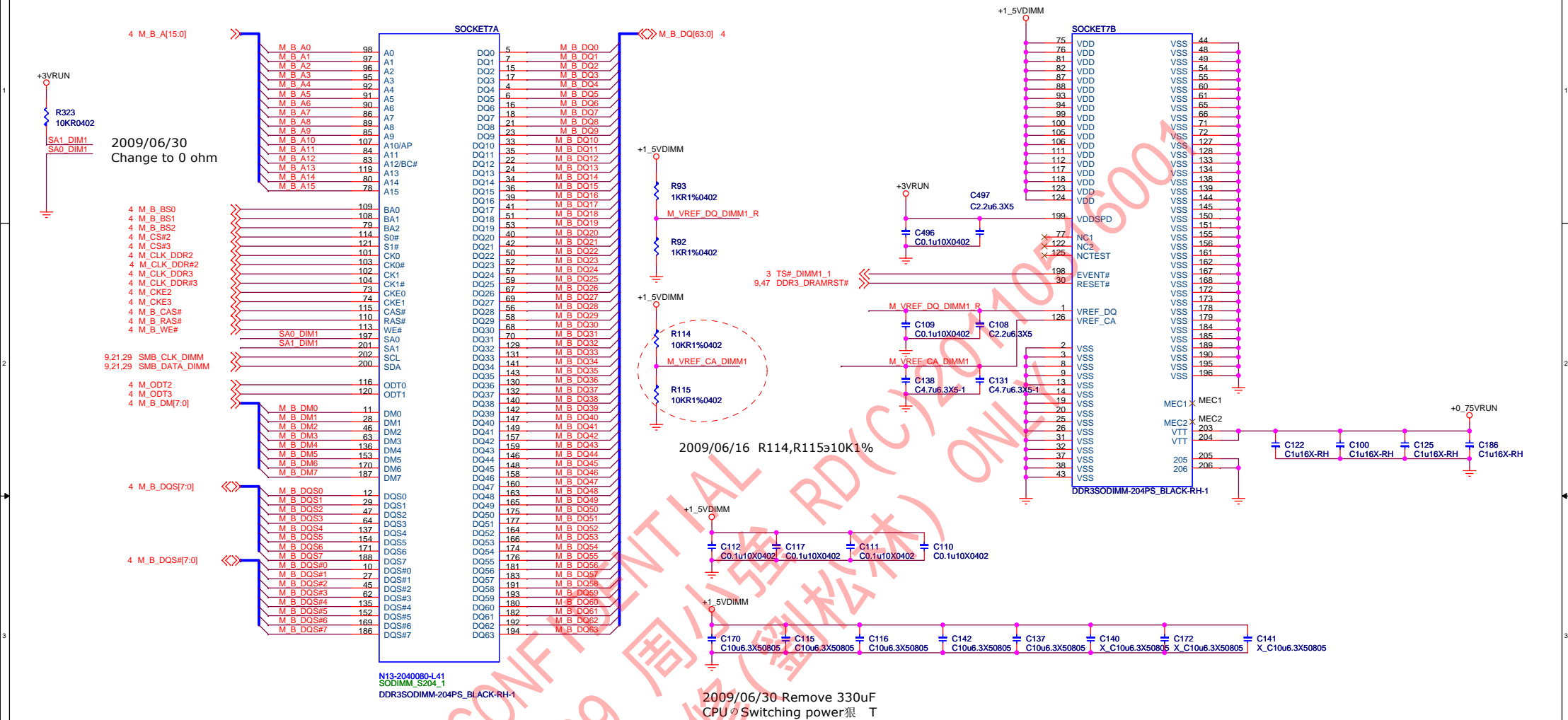


Layout Note:
Location of all CFG strap resistors needs
to be close to trace to minimize stub

SODIMM#A



SODIMM#B



2009/06/30 緯 CPU(TX)

PEG_TXP0	C555	C0.1u10X0402	GFX_RXP0	AF30	PCIE_RX0P
PEG_TXN0	C557	C0.1u10X0402	GFX_RXN0	AE31	PCIE_RX0N
PEG_TXP1	C559	C0.1u10X0402	GFX_RXP1	AE29	PCIE_RX1P
PEG_TXN1	C561	C0.1u10X0402	GFX_RXN1	AD28	PCIE_RX1N
PEG_TXP2	C563	C0.1u10X0402	GFX_RXP2	AD30	PCIE_RX2P
PEG_TXN2	C564	C0.1u10X0402	GFX_RXN2	AC31	PCIE_RX2N
PEG_TXP3	C565	C0.1u10X0402	GFX_RXP3	AC29	PCIE_RX3P
PEG_TXN3	C566	C0.1u10X0402	GFX_RXN3	AB28	PCIE_RX3N
PEG_TXP4	C567	C0.1u10X0402	GFX_RXP4	AB30	PCIE_RX4P
PEG_TXN4	C570	C0.1u10X0402	GFX_RXN4	AA31	PCIE_RX4N
PEG_TXP5	C572	C0.1u10X0402	GFX_RXP5	AA29	PCIE_RX5P
PEG_TXN5	C573	C0.1u10X0402	GFX_RXN5	Y28	PCIE_RX5N
PEG_TXP6	C574	C0.1u10X0402	GFX_RXP6	Y30	PCIE_RX6P
PEG_TXN6	C575	C0.1u10X0402	GFX_RXN6	W31	PCIE_RX6N
PEG_TXP7	C576	C0.1u10X0402	GFX_RXP7	W29	PCIE_RX7P
PEG_TXN7	C586	C0.1u10X0402	GFX_RXN7	V28	PCIE_RX7N
PEG_TXP8	C587	C0.1u10X0402	GFX_RXP8	V30	PCIE_RX8P
PEG_TXN8	C588	C0.1u10X0402	GFX_RXN8	U31	PCIE_RX8N
PEG_TXP9	C596	C0.1u10X0402	GFX_RXP9	U29	PCIE_RX9P
PEG_TXN9	C595	C0.1u10X0402	GFX_RXN9	T28	PCIE_RX9N
PEG_TXP10	C585	C0.1u10X0402	GFX_RXP10	T30	PCIE_RX10P
PEG_TXN10	C584	C0.1u10X0402	GFX_RXN10	R31	PCIE_RX10N
PEG_TXP11	C594	C0.1u10X0402	GFX_RXP11	R29	PCIE_RX11P
PEG_TXN11	C593	C0.1u10X0402	GFX_RXN11	P28	PCIE_RX11N
PEG_TXP12	C583	C0.1u10X0402	GFX_RXP12	P30	PCIE_RX12P
PEG_TXN12	C582	C0.1u10X0402	GFX_RXN12	N31	PCIE_RX12N
PEG_TXP13	C592	C0.1u10X0402	GFX_RXP13	N29	PCIE_RX13P
PEG_TXN13	C591	C0.1u10X0402	GFX_RXN13	M28	PCIE_RX13N
PEG_TXP14	C581	C0.1u10X0402	GFX_RXP14	M30	PCIE_RX14P
PEG_TXN14	C580	C0.1u10X0402	GFX_RXN14	L31	PCIE_RX14N
PEG_TXP15	C590	C0.1u10X0402	GFX_RXP15	L29	PCIE_RX15P
PEG_TXN15	C589	C0.1u10X0402	GFX_RXN15	K30	PCIE_RX15N

U40A

PCI EXPRESS INTERFACE

PCIE_TX0P	AH30	GFX_TXP0	C260	C0.1u10X0402	PEG_RXP0
PCIE_TX0N	AG31	GFX_TXN0	C264	C0.1u10X0402	PEG_RXN0
PCIE_TX1P	AG29	GFX_TXP1	C267	C0.1u10X0402	PEG_RXP1
PCIE_TX1N	AF28	GFX_TXN1	C263	C0.1u10X0402	PEG_RXN1
PCIE_TX2P	AF27	GFX_TXP2	C272	C0.1u10X0402	PEG_RXP2
PCIE_TX2N	AF26	GFX_TXN2	C268	C0.1u10X0402	PEG_RXN2
PCIE_TX3P	AD27	GFX_TXP3	C271	C0.1u10X0402	PEG_RXP3
PCIE_TX3N	AD26	GFX_TXN3	C276	C0.1u10X0402	PEG_RXN3
PCIE_TX4P	AC25	GFX_TXP4	C287	C0.1u10X0402	PEG_RXP4
PCIE_TX4N	AB25	GFX_TXN4	C283	C0.1u10X0402	PEG_RXN4
PCIE_TX5P	Y23	GFX_TXP5	C286	C0.1u10X0402	PEG_RXP5
PCIE_TX5N	Y24	GFX_TXN5	C291	C0.1u10X0402	PEG_RXN5
PCIE_TX6P	AB27	GFX_TXP6	C295	C0.1u10X0402	PEG_RXP6
PCIE_TX6N	AB26	GFX_TXN6	C299	C0.1u10X0402	PEG_RXN6
PCIE_TX7P	Y27	GFX_TXP7	C298	C0.1u10X0402	PEG_RXP7
PCIE_TX7N	Y26	GFX_TXN7	C302	C0.1u10X0402	PEG_RXN7
PCIE_TX8P	W24	GFX_TXP8	C304	C0.1u10X0402	PEG_RXP8
PCIE_TX8N	W23	GFX_TXN8	C313	C0.1u10X0402	PEG_RXN8
PCIE_TX9P	Y27	GFX_TXP9	C307	C0.1u10X0402	PEG_RXP9
PCIE_TX9N	U26	GFX_TXN9	C314	C0.1u10X0402	PEG_RXN9
PCIE_TX10P	U24	GFX_TXP10	C318	C0.1u10X0402	PEG_RXP10
PCIE_TX10N	U23	GFX_TXN10	C323	C0.1u10X0402	PEG_RXN10
PCIE_TX11P	T26	GFX_TXP11	C322	C0.1u10X0402	PEG_RXP11
PCIE_TX11N	T27	GFX_TXN11	C325	C0.1u10X0402	PEG_RXN11
PCIE_TX12P	T24	GFX_TXP12	C329	C0.1u10X0402	PEG_RXP12
PCIE_TX12N	T23	GFX_TXN12	C333	C0.1u10X0402	PEG_RXN12
PCIE_TX13P	P27	GFX_TXP13	C332	C0.1u10X0402	PEG_RXP13
PCIE_TX13N	P26	GFX_TXN13	C336	C0.1u10X0402	PEG_RXN13
PCIE_TX14P	P24	GFX_TXP14	C343	C0.1u10X0402	PEG_RXP14
PCIE_TX14N	P23	GFX_TXN14	C347	C0.1u10X0402	PEG_RXN14
PCIE_TX15P	M27	GFX_TXP15	C348	C0.1u10X0402	PEG_RXP15
PCIE_TX15N	N26	GFX_TXN15	C345	C0.1u10X0402	PEG_RXN15

PEG_RXN[15:0] << PEG_RXN[15:0] 3
PEG_RXP[15:0] << PEG_RXP[15:0] 3
PEG_TXP[15:0] >> PEG_TXP[15:0] 3
PEG_TXN[15:0] >> PEG_TXN[15:0] 3

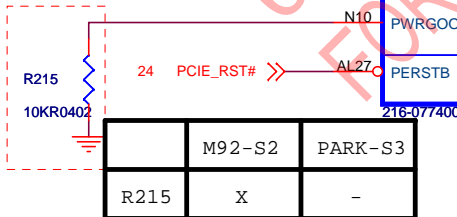
21 CLK_PEGA_MXM_P >> AK30
21 CLK_PEGA_MXM_N >> AK32

CLOCK
PCIE_REFCLKP
PCIE_REFCLKN

CheckResetSequence

For Park-S3: PWRGOOD pin must need to pull low


For M92-S2/S3: PWRGOOD pin should be NC



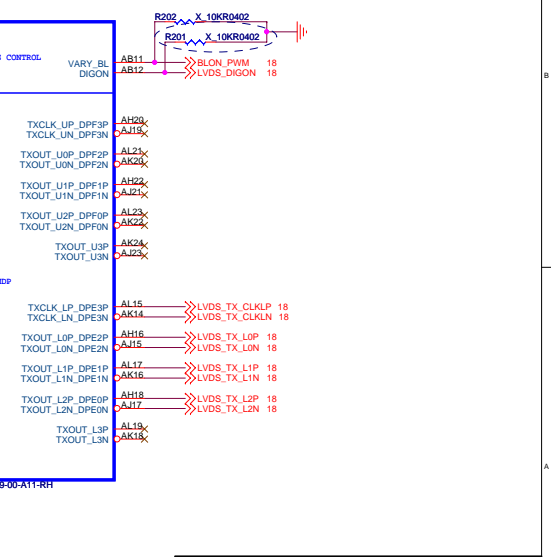
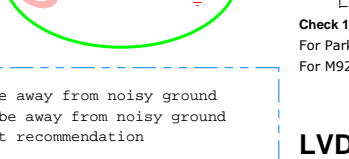
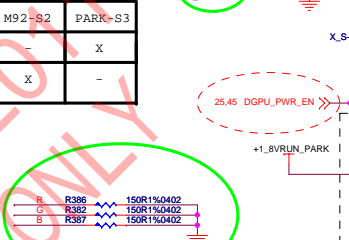
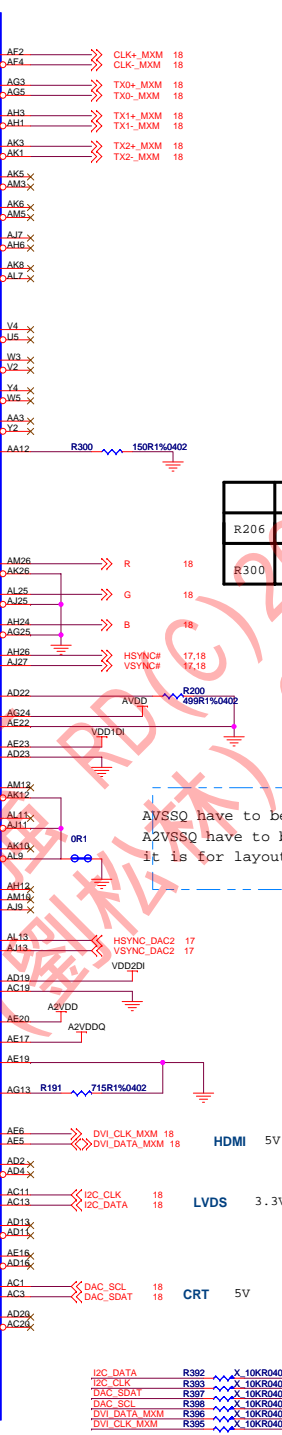
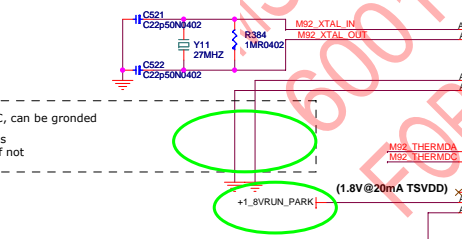
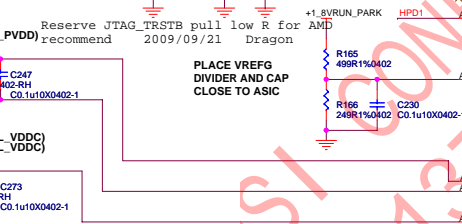
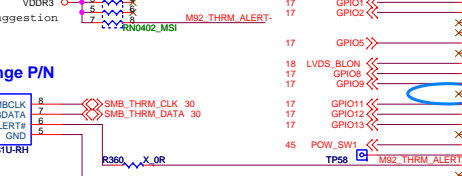
CALIBRATION

PCIE_CALRP Y22 VGA PE CP R203 1.27KΩ
PCIE_CALRN AA22 VGA PE CN R205 2KΩ 0402 +1.0V RUN_PARK

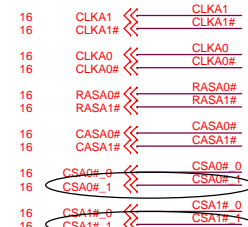
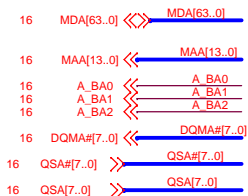
216-0774009-00-A11-RH

			MICRO-STAR INT'L CO.,LTD.		
Title M92/Pak-Sx (PCIE Interface)					
Size	Document Number				Rev
Custom	MS-145X				10
Date:	Wednesday, November 18, 2009		Sheet	11	of 56

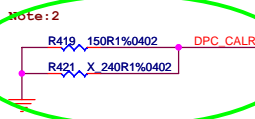
```
For PARK-S3: Install All components in this
Box INCLUDING Decoupling caps and Bead
connecting to DPC_VDD18#
|
For M92-S2: DO NOT Install any Component
in this Box.
```



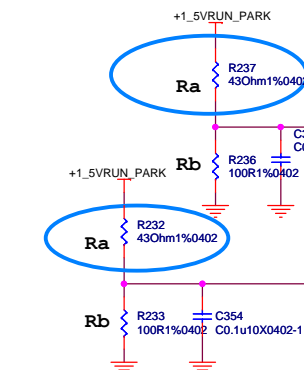
MVDDQ = 1.5V FOR DDR3 Memory



	M92-S2	PARK-S3
R419	X	-
R421	-	X



PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC



	M92-S2	PARK-S3
R428	-	X
R226	-	X

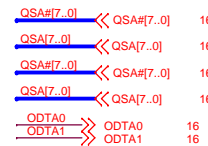
DIVIDER RESISTORS	DDR3
MVREF TO 1.5V (Ra)	43R
MVREF TO GND (Rb)	100R

DDR3 Memory Interface



route 50ohms
single-ended/100ohms diff
and keep short
Use this option ONLY
for Park-S3

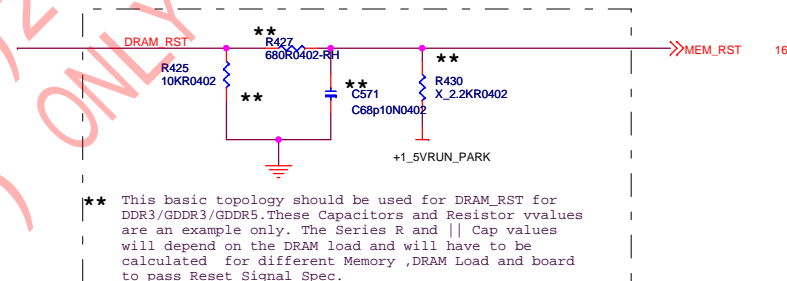
	M92-S2	PARK-S3
C568	X	-
C341	X	-
R423	X	-
R227	X	-



	M92-S2	PARK-S3
R247	X	-
R246	X	-

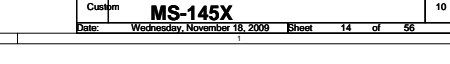
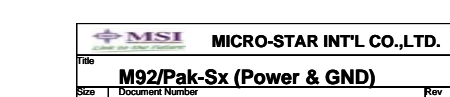
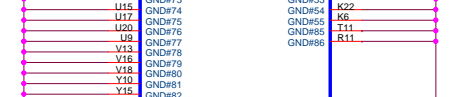
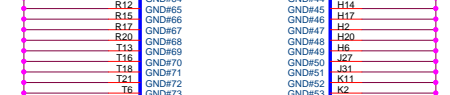
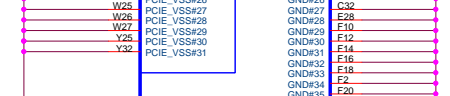
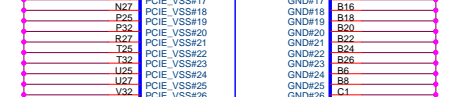
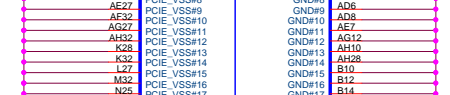
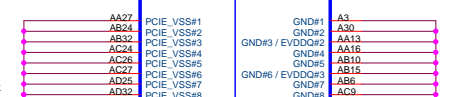
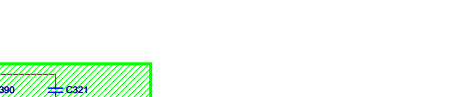
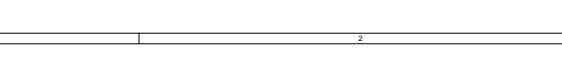
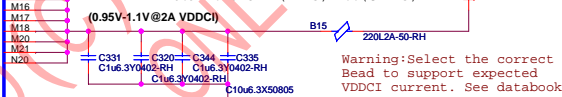
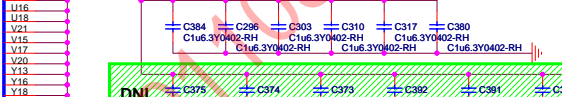
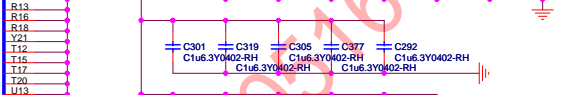
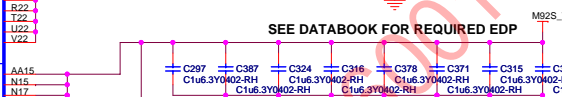
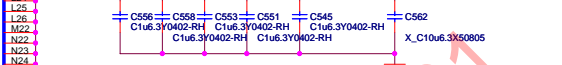
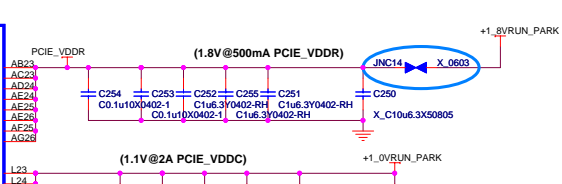
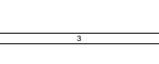
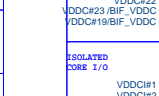
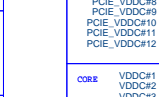
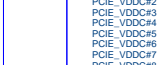
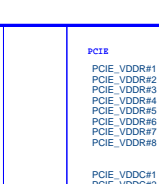
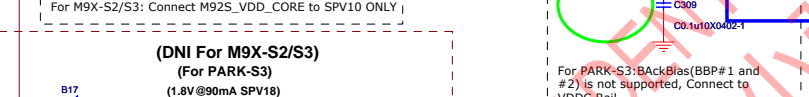
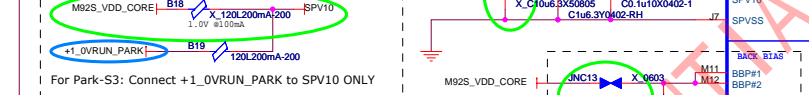
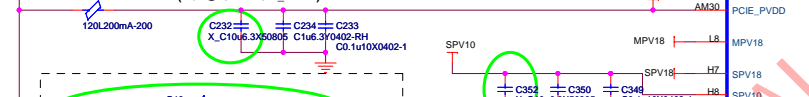
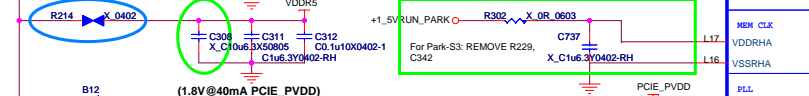
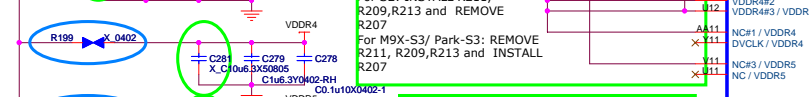
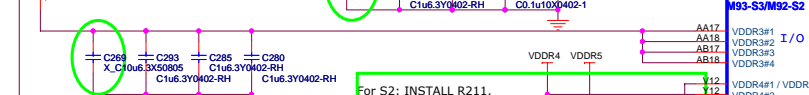
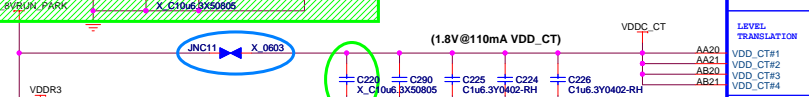
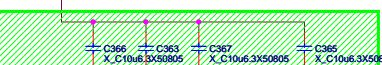
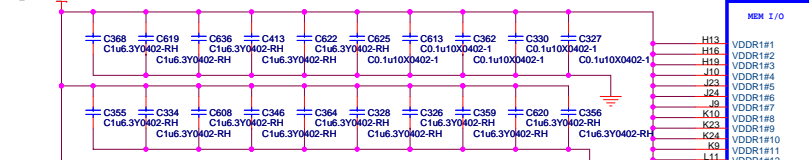


- Note 1 : Do not Install for M9X-S2/S3, Install 240 Ohms 0.5% Resistor for PARK-S3.
 Note 2 : For M9X-S2/S3, J8 Pin Connect to VSS through 240 Ohms(0.5%) resistor.
 For Park-S3, J8 Pin Connect to VSS through 150 Ohms(1%) resistor for DPC_CALR
 Note 3 : For M9X-92/93, K7 Pin (NC_MEM_CALRP1) is Not connected.
 For PARK-S3, K7 Pin (TESTEN#2) connect to TEST_EN Signal At AF24



Designator	For M9X-S2 and M93-S3	For Park-S3
R425	DNI	10K
R427	0R/Short	680R
R430	2.2K	DNI
C571	2.2nF	68pF

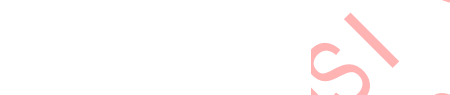
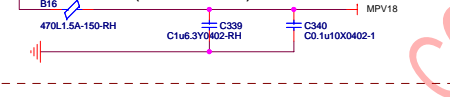
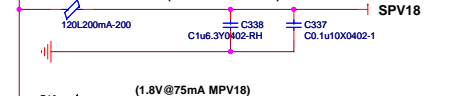
(for DDR2 and GDDR3: 1.8V@2.2A VDDR1) (For DDR3, MVDDQ = 1.5V@2.0A)



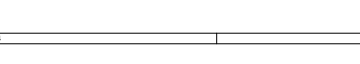
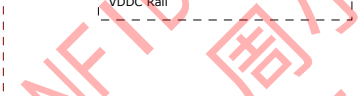
	M92-S2	PARK-S3
R211	-	X
R207	X	-
R209	-	X
R213	-	X

	M92-S2	PARK-S3
B18	-	X
B19	X	-

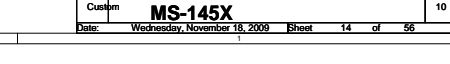
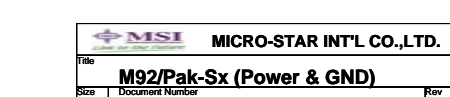
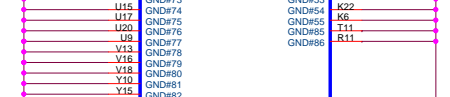
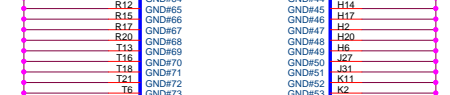
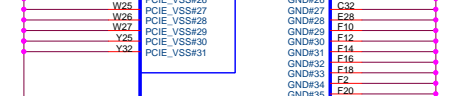
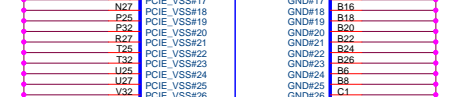
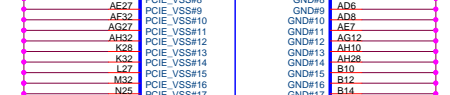
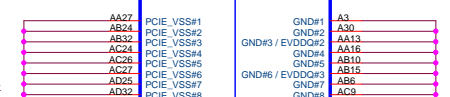
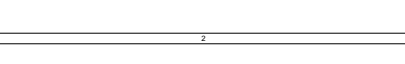
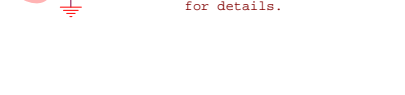
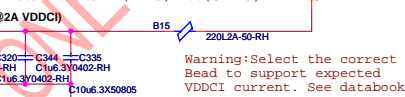
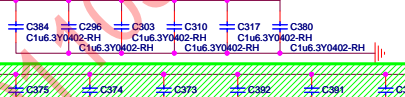
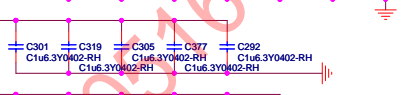
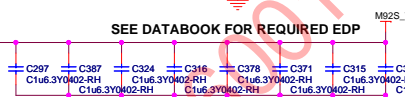
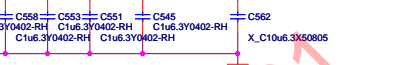
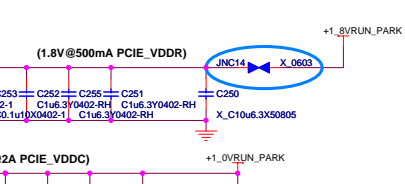
(DNI For M9X-S2/S3)
(For PARK-S3)
(1.8V@90mA SPV18)



(DNI For M9X-S2/S3)
(For PARK-S3)
(1.8V@75mA MPV18)



(DNI For M9X-S2/S3)
(For PARK-S3)
(1.8V@110mA VDD_CT)



**LVDS Mode: 1.8V@200mA
(DP Mode: 1.8V@130mA)**

B11 470L1.5A-150-RH C237 X_C10u6.3X50805 C258 C1u6.3Y0402-RH C246 C0.1u10X0402-1

DPE_VDD18

(1.8V@20mA)

B21 120L200mA-200 C514 X_C10u6.3X50805 C516 C1u6.3Y0402-RH C520 C0.1u10X0402-1

DPE_PVDD

[illegible]

Park-S3: 110mA@1.0V
M9X-S2/S3: 200mA@1.1V

DPA_VDD10

B13 120L600mA-250

C239 10uF
X_C10 6.3X50805
C245 6.3Y0402-RH
C244 0.1uF
C01 0.1X0402-1

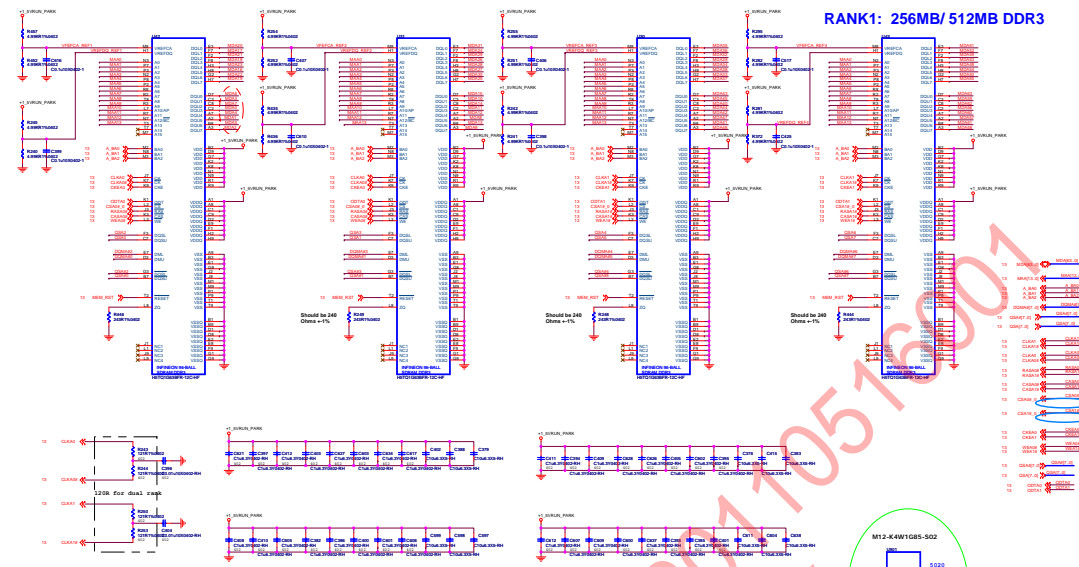
+1.0V RUN_PARK

Park-S3: TMDS/DP=110mA@1.0V ; LVDS=120mA@1.0V
M9X-S2/S3: TMDS/DP=170mA@1.1V LVDS=100mA@1.1V

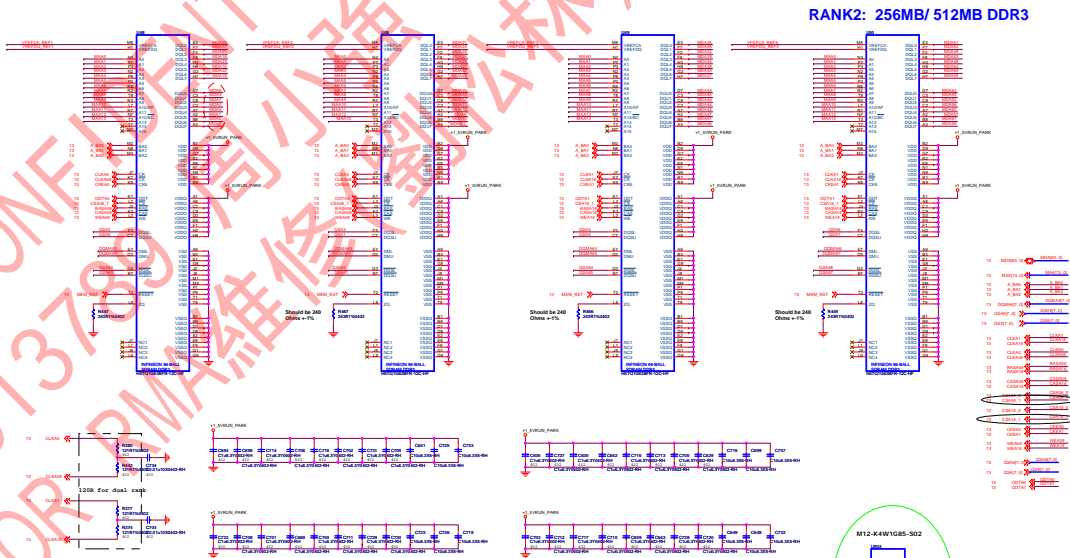
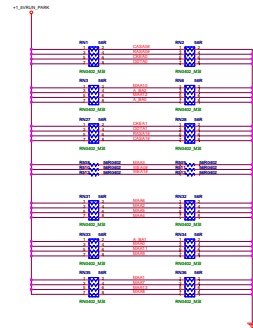
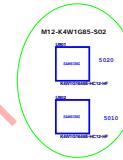
DPE_VDD10

B20 120L600mA-250

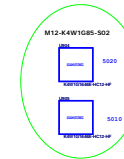
C519 10uF
X_C10 6.3X50805
C519 6.3Y0402-RH
C515 0.1uF
C01 0.1X0402-1



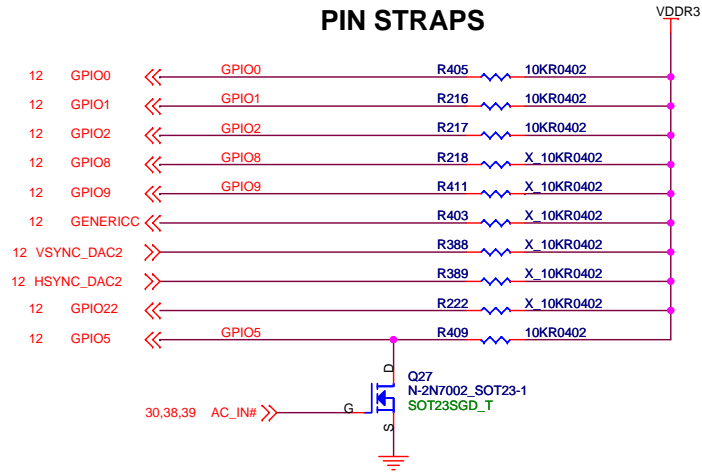
For M9X-S2/S3 with DDR3: Support MAA12-MAA0 Address or 64MX16 DDR3. MAA13 is NC
For PARK-S3 with DDR3: Support MAA13-MAA0 Address or 128MX16 DDR3.



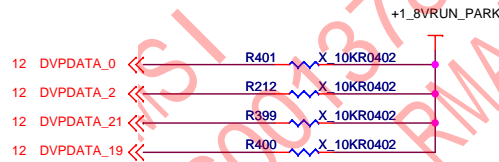
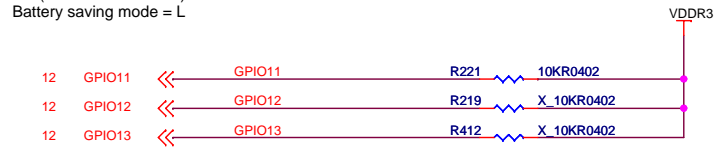
For M9X-S2/S3 with DDR3: Support MAA12-MAA0 Address or 64MX16 DDR3. MAA13 is NC
For PARK-S3 with DDR3: Support MAA13-MAA0 Address or 128MX16 DDR3.



PIN STRAPS



GPIO_5_AC_BATT is an optional input which allows the system to request (AC) performance mode or battery mode operation.
AC (Performance mode) = H
Battery saving mode = L




CONFIGURATION STRAPS

PIN	M92-S2 LP	PARK LP S3	DESCRIPTION OF DEFAULT SETTINGS
GPIO0	1		GPIO=0 50% TX output swing GPIO=1 Full TX output swing
GPIO1	1		GPIO=0 TX de-emphasis disabled GPIO=1 TX de-emphasis enabled
GPIO2	1		GPIO=0 Advertises the PCIe device as 2.5 GT/S capable at power-on GPIO=1 Advertises the PCIe device as 5 GT/S capable at power-on
GPIO9	0		GPIO=0 VGA controller capacity enabled. GPIO=1 The device will not be recognized as the system's VGA controller.
VSYNC_DAC2	0		GPIO=0 Driver would ignore the value sampled on DVPDATA_20 during reset.
GPIO22	0		GPIO=0 not used external BIOS ROM GPIO=1 if used

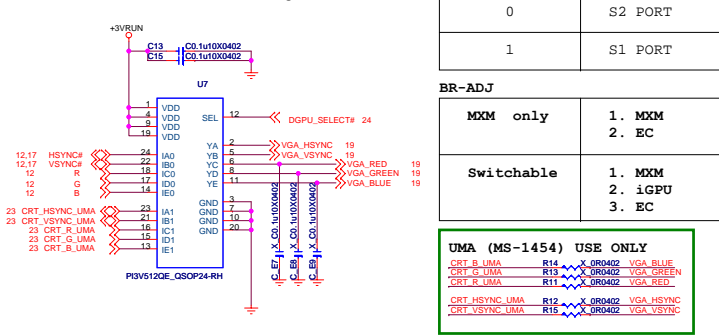
PIN	M92-S2 LP	PARK LP S3	DESCRIPTION OF DEFAULT SETTINGS
GPIO 13 GPIO 12 GPIO 11	0 0 1		0 0 0=128 MB 0 0 1=256 MB 0 1 0=64 MB

PIN	M92-S2 LP	PARK LP S3	DESCRIPTION OF DEFAULT SETTINGS
VGA_HSYNC# VGA_VSYNC#	1 1		0 0=No audio function 0 1=Audio for display port only 1 0=Audio for display port and HDMI if dongle is detected 1 1=Audio for both displayport and HDMI

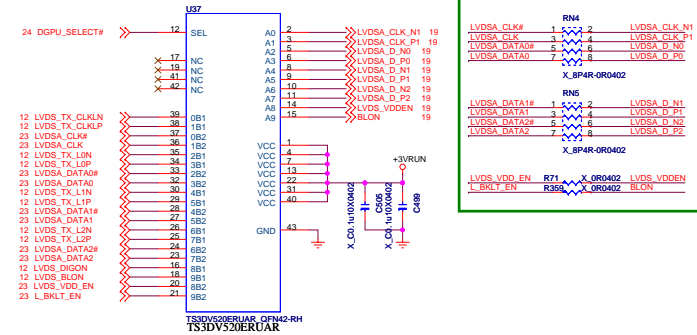
DVPDATA19	DVPDATA21	DVPDATA2	DVPDATA0	MEM_TYPE
0	0	0	0	Hynix 64Mx16 DDR3 (M12-5TQ1G25-H23)
0	0	0	1	Samsung 64Mx16 DDR3 (M12-K4W1G85-S02)
0	0	1	0	
0	0	1	1	

 MSI <small>MOBILE SYSTEMS INTERNATIONAL</small>		MICRO-STAR INT'L CO.,LTD.	
Title			
M92/Pak-Sx (Straps & Thermal)			
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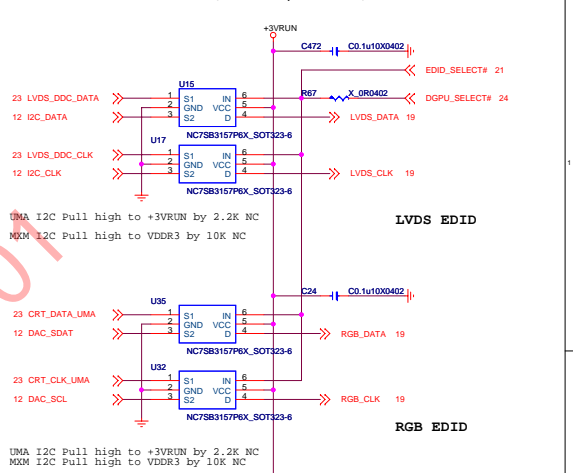
CRT Switch



LVDS Switch

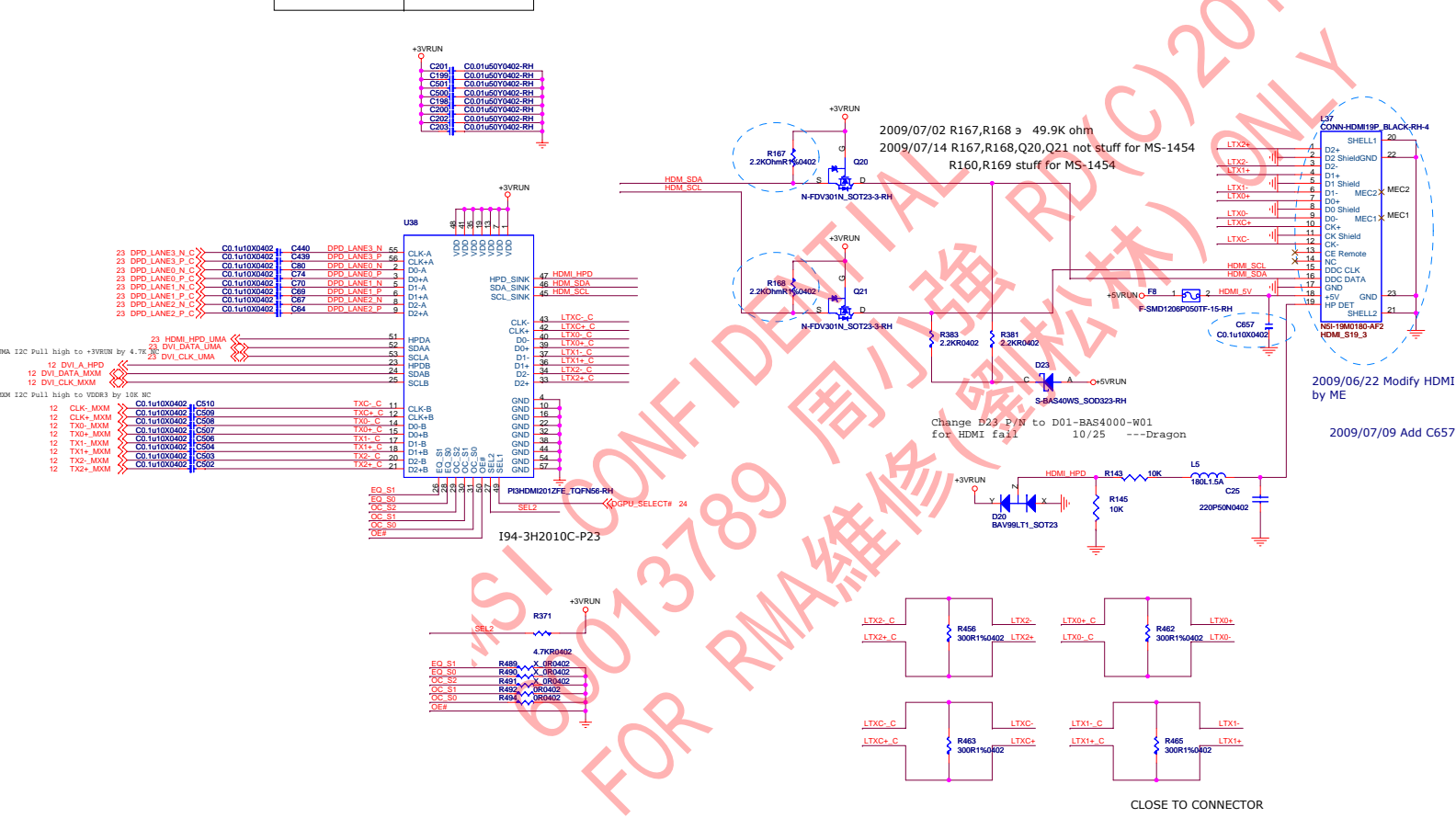


EDID Switch (CRT, LVDS)

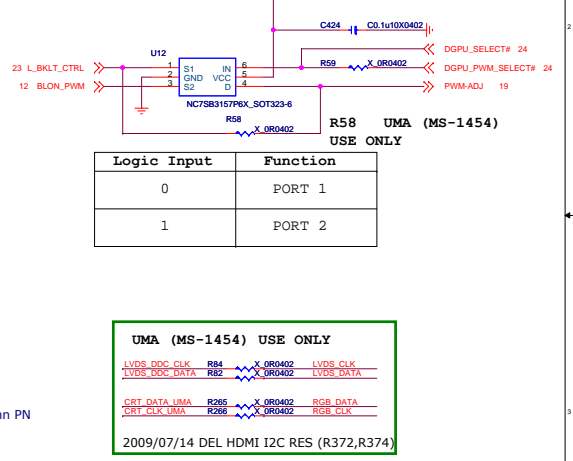


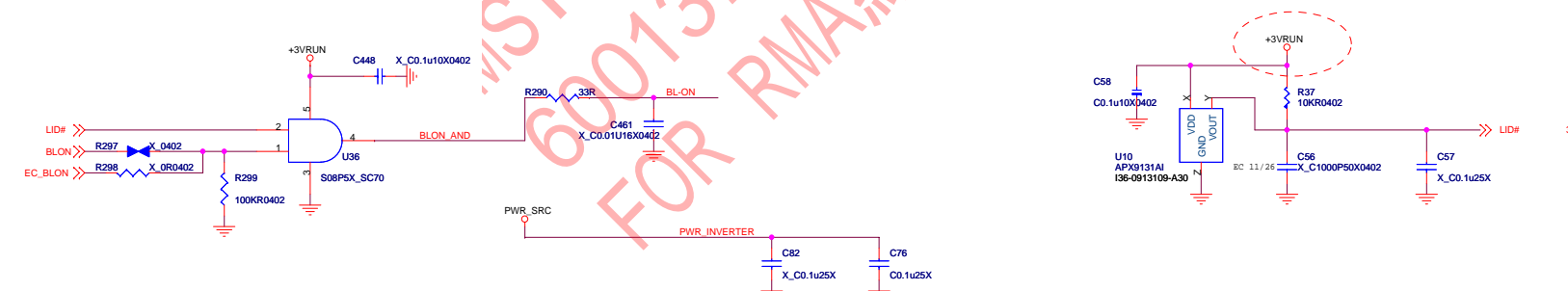
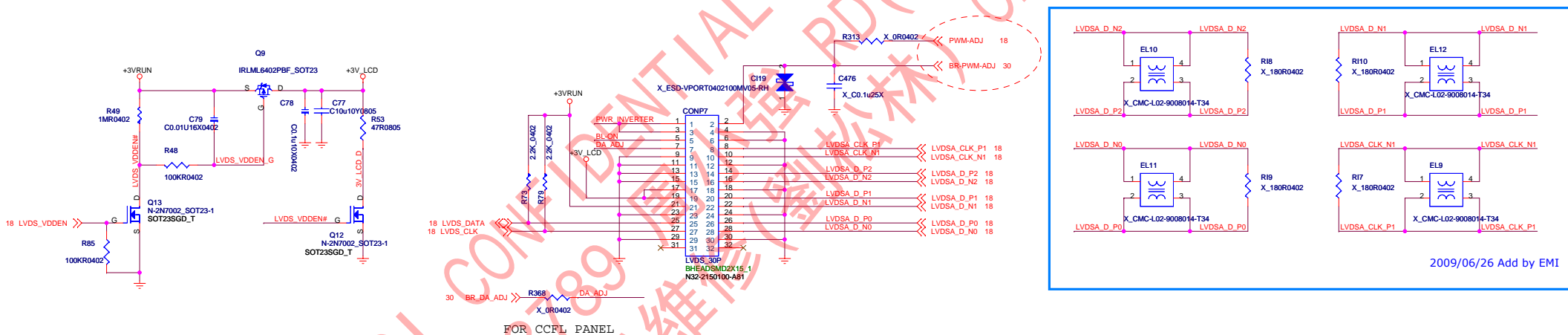
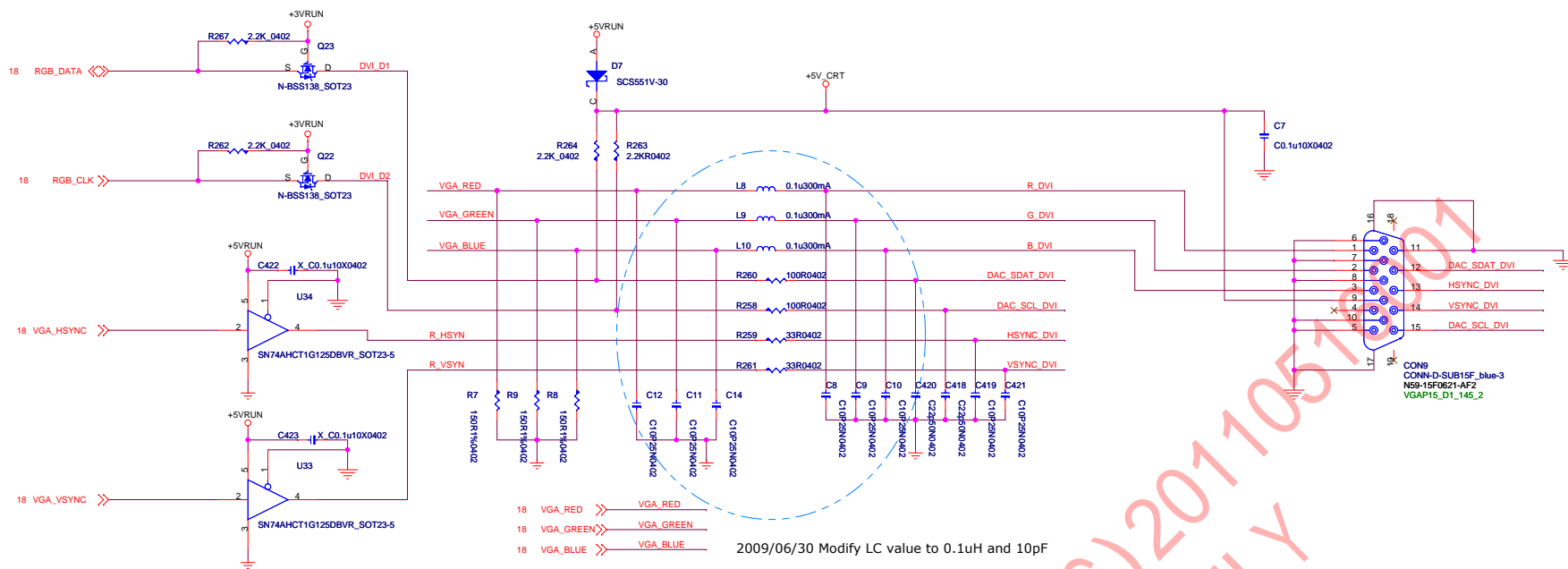
HDMI Switch

2009/07/14 Change HDMI SW

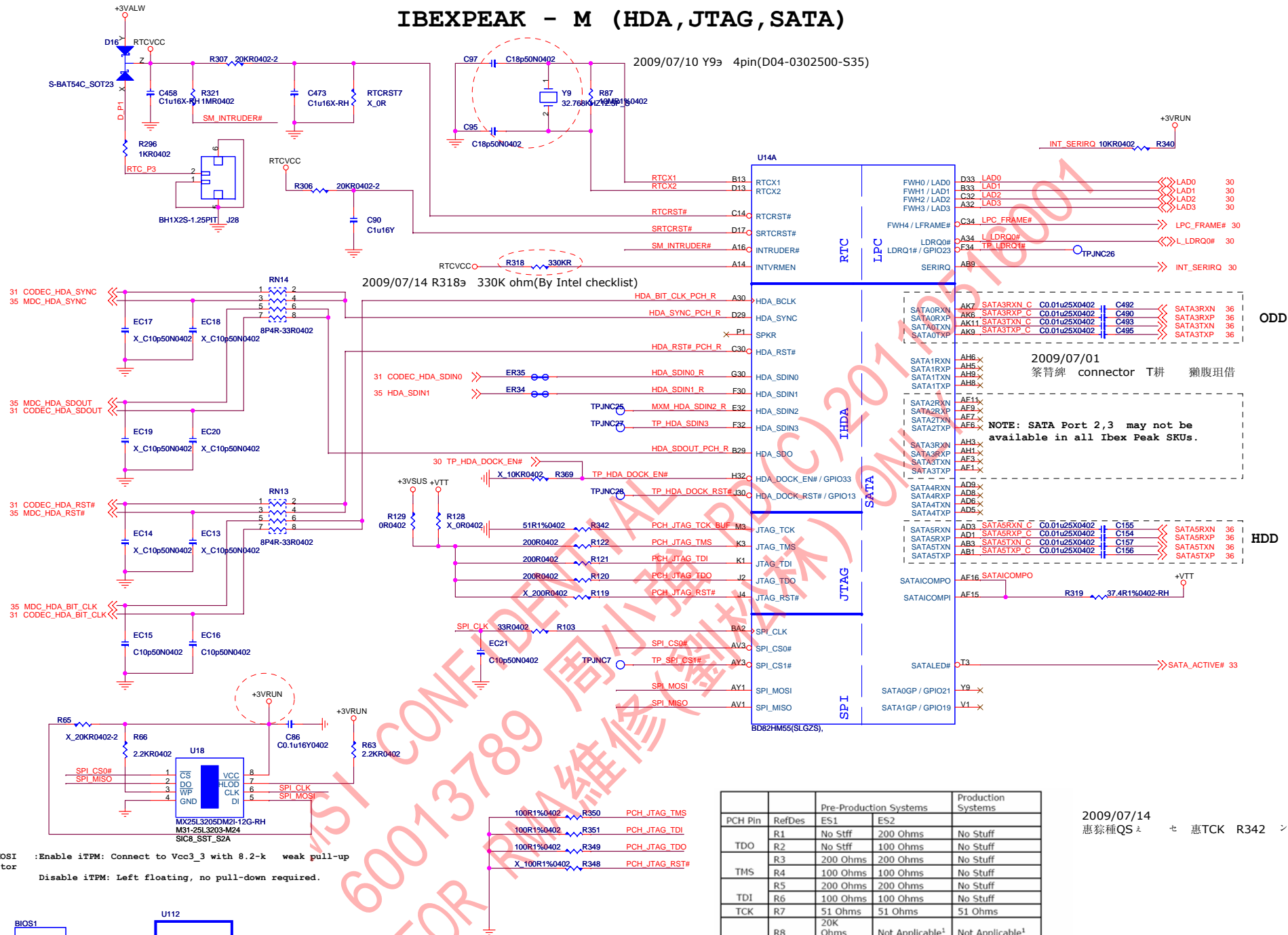


2009/07/14 DEL HDMI I2C SW (U26, U27)





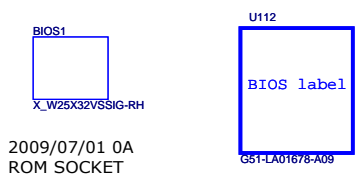
IBEXPEAK - M (HDA, JTAG, SATA)



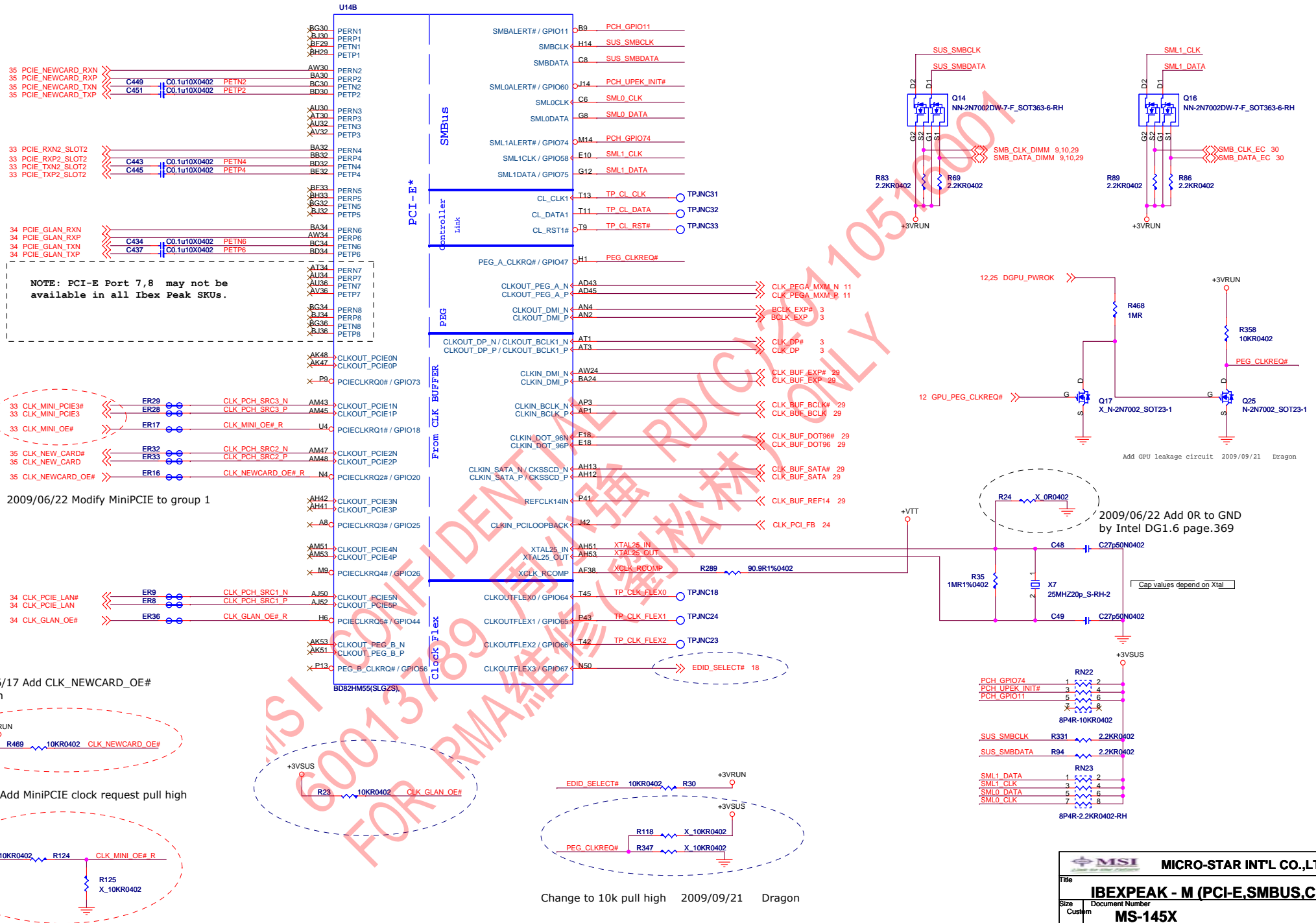
PCH Pin	RefDes	Pre-Production Systems		Production Systems
		ES1	ES2	
TDO	R1	No Stff	200 Ohms	No Stuff
	R2	No Stff	100 Ohms	No Stuff
TMS	R3	200 Ohms	200 Ohms	No Stuff
	R4	100 Ohms	100 Ohms	No Stuff
	R5	200 Ohms	200 Ohms	No Stuff
TDI	R6	100 Ohms	100 Ohms	No Stuff
TCK	R7	51 Ohms	51 Ohms	51 Ohms
	R8	20K Ohms	Not Applicable ¹	Not Applicable ¹
TRST#	R9	10K Ohms	Not Applicable ¹	Not Applicable ¹

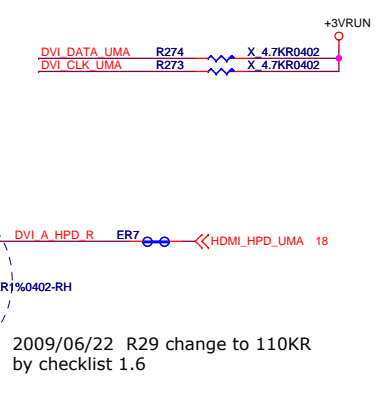
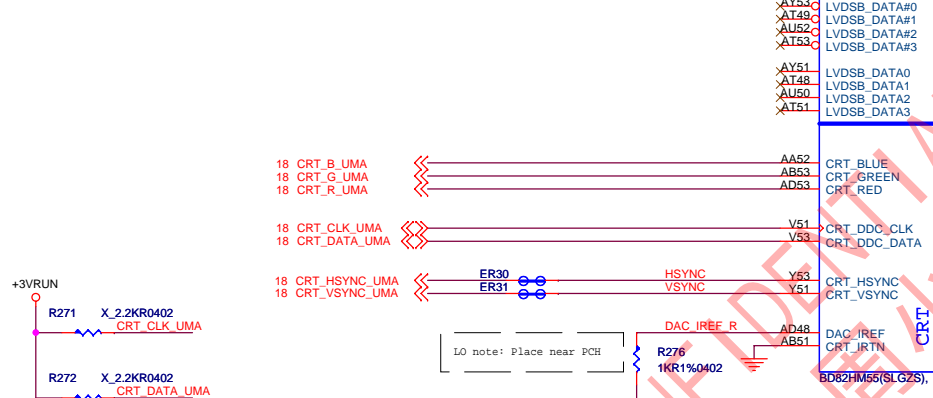
Note 1: For IBX ES2 and later, TRST# does not require an external pull-up; but should be routed to a test point pad for PCH JTAG debug purposes


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IBEXPEAK - M (HDA,JTAG,SATA)	
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IBEXPEAK - M (PCI-E, SMBUS, CLK)



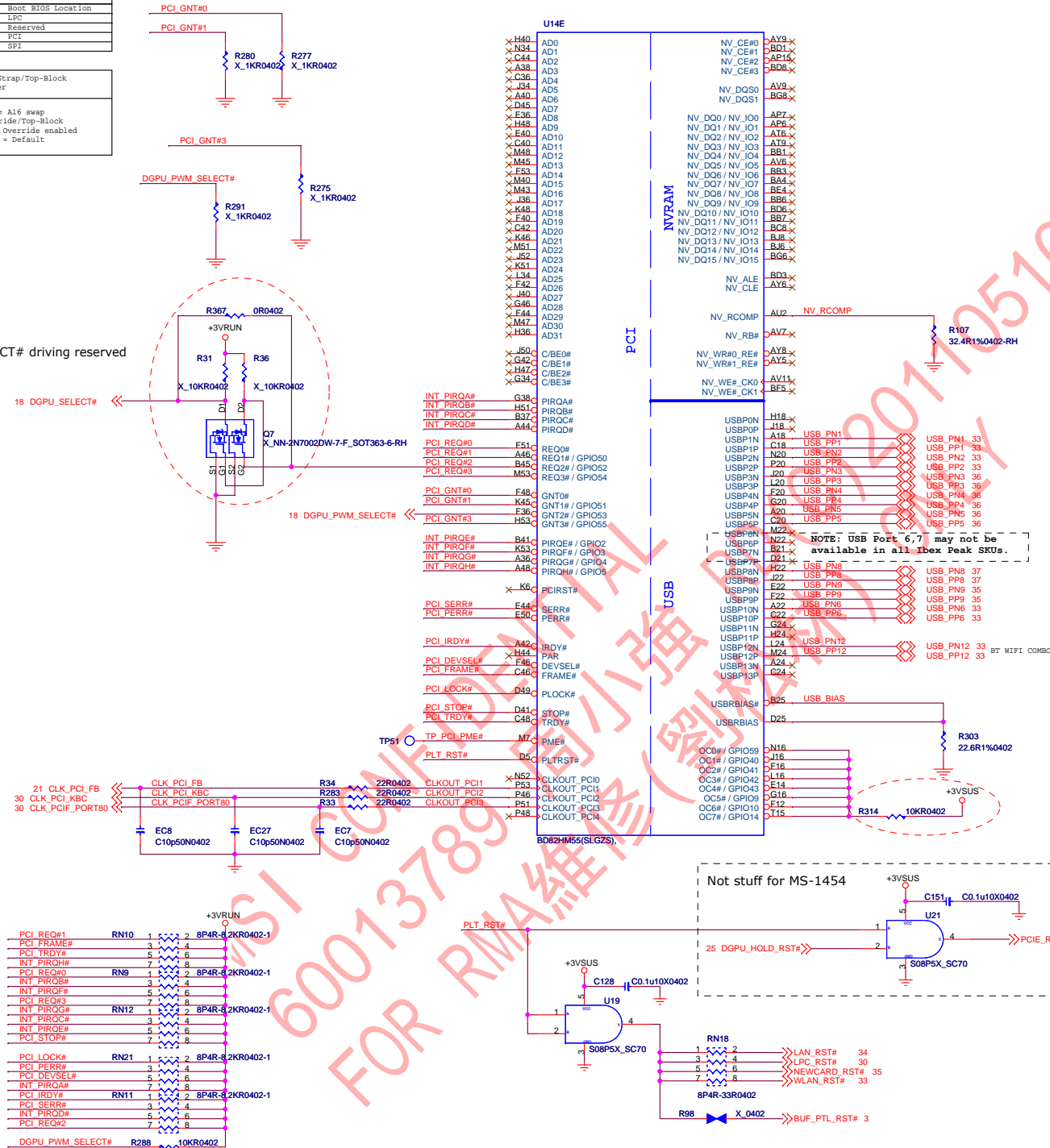


 MICRO-STAR INT'L CO.,LTD.	
IBEXPEAK - M (LVDS,DDI)	
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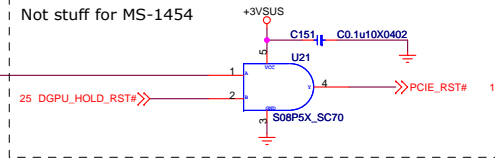
IBEXPEAK - M (PCI,USB,NVRAM)

Boot BIOS Strap		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default



Not stuff for MS-1454

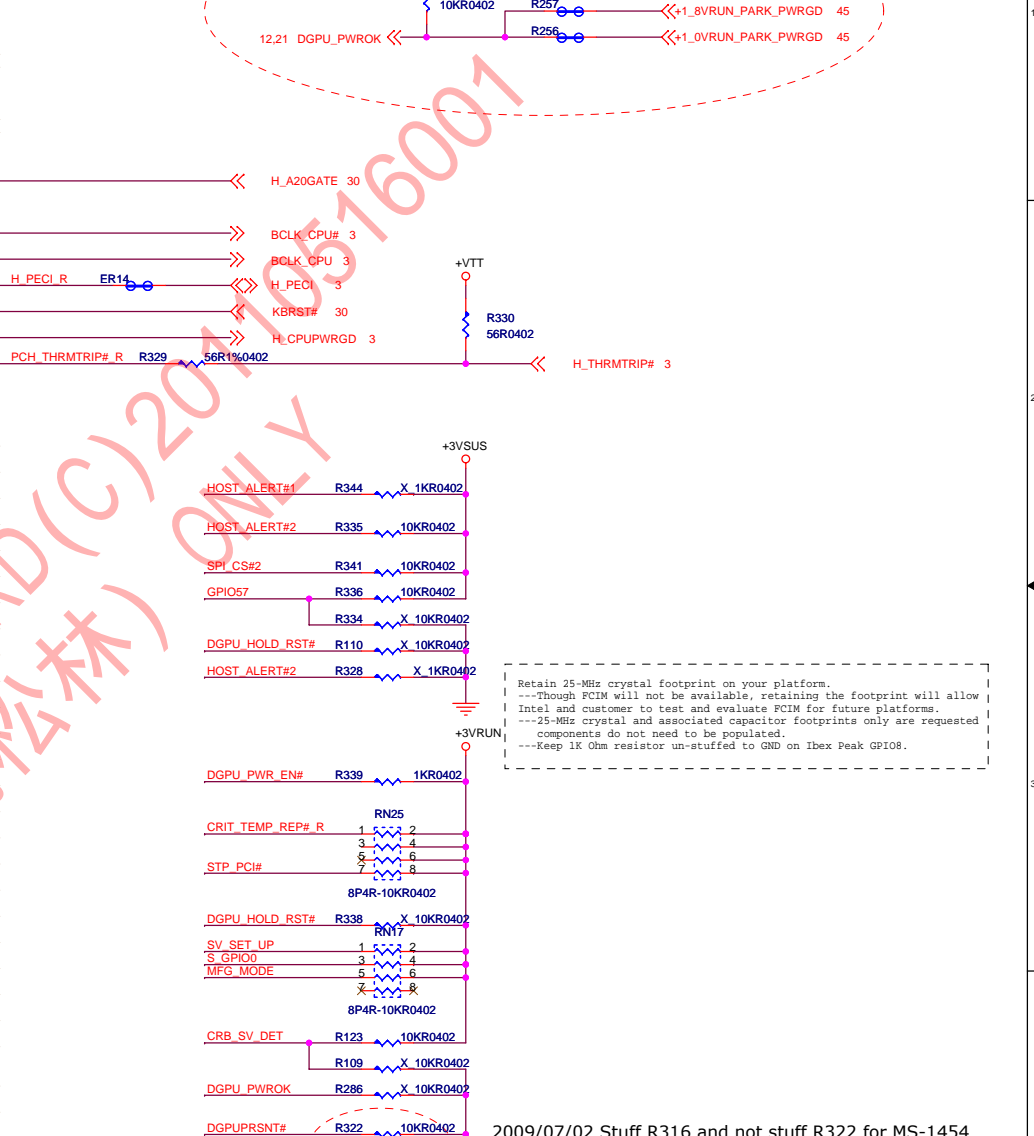
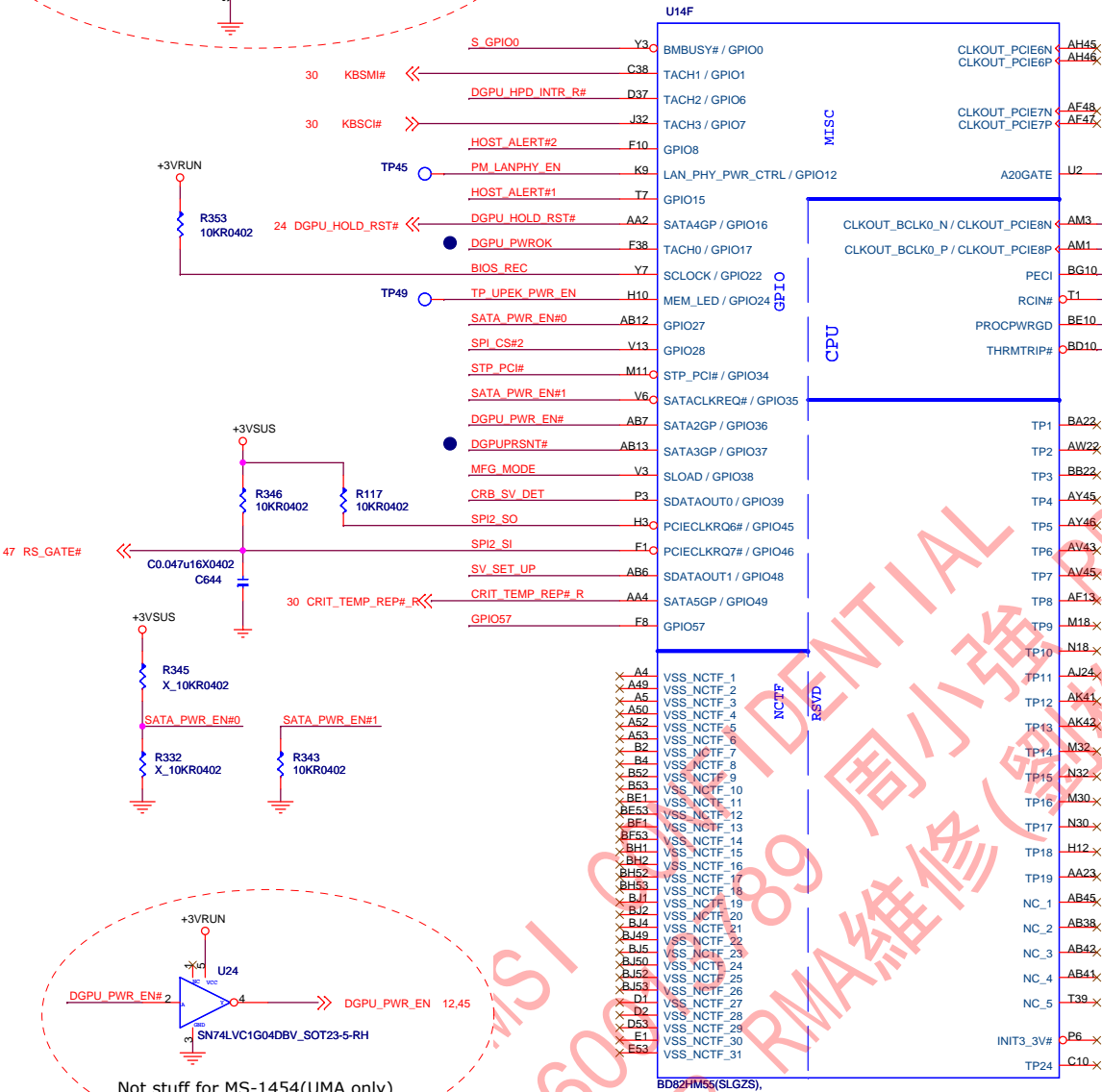
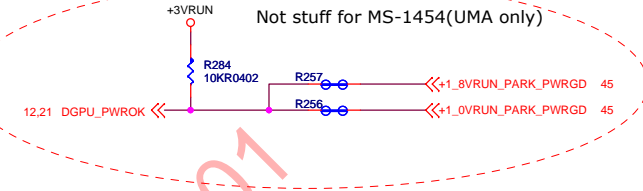
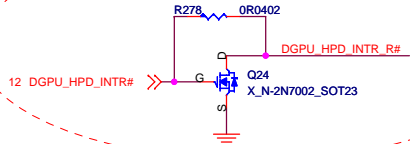


RN18
 1 2
 3 4
 5 6
 7 8
 8P4R-33R0402
 3 X_0402
 LAN_RST# 34
 LPC_RST# 30
 NEWCARD_RST# 35
 WLAN_RST# 33
 BUF_PTL_RST# 3

IBEXPEAK - M (GPIO,VSS_NCTF,RSVD)

2009/07/01 Combine Park 1.8V and 1.0V to DGPU_PWROK

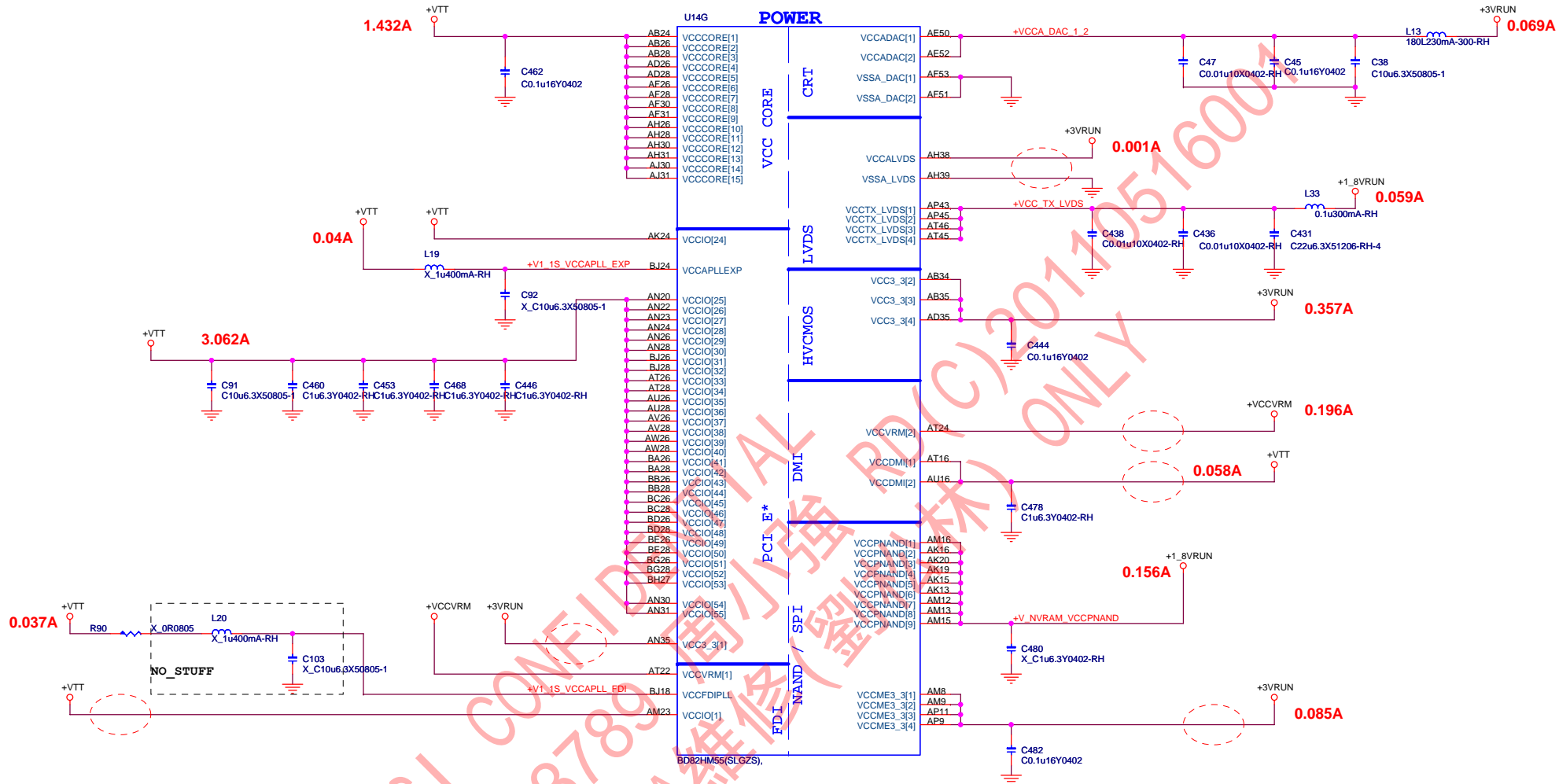
Not stuff for MS-1454(UMA only)



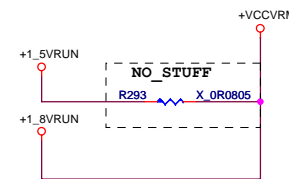
Retain 25-MHz crystal footprint on your platform.
 ---Though FCIM will not be available, retaining the footprint will allow Intel and customer to test and evaluate FCIM for future platforms.
 ---25-MHz crystal and associated capacitor footprints only are requested components do not need to be populated.
 ---Keep 1K Ohm resistor un-stuffed to GND on Ibox Peak GPIO8.

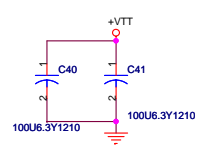
2009/07/02 Stuff R316 and not stuff R322 for MS-1454

IBEXPEAK - M (POWER)

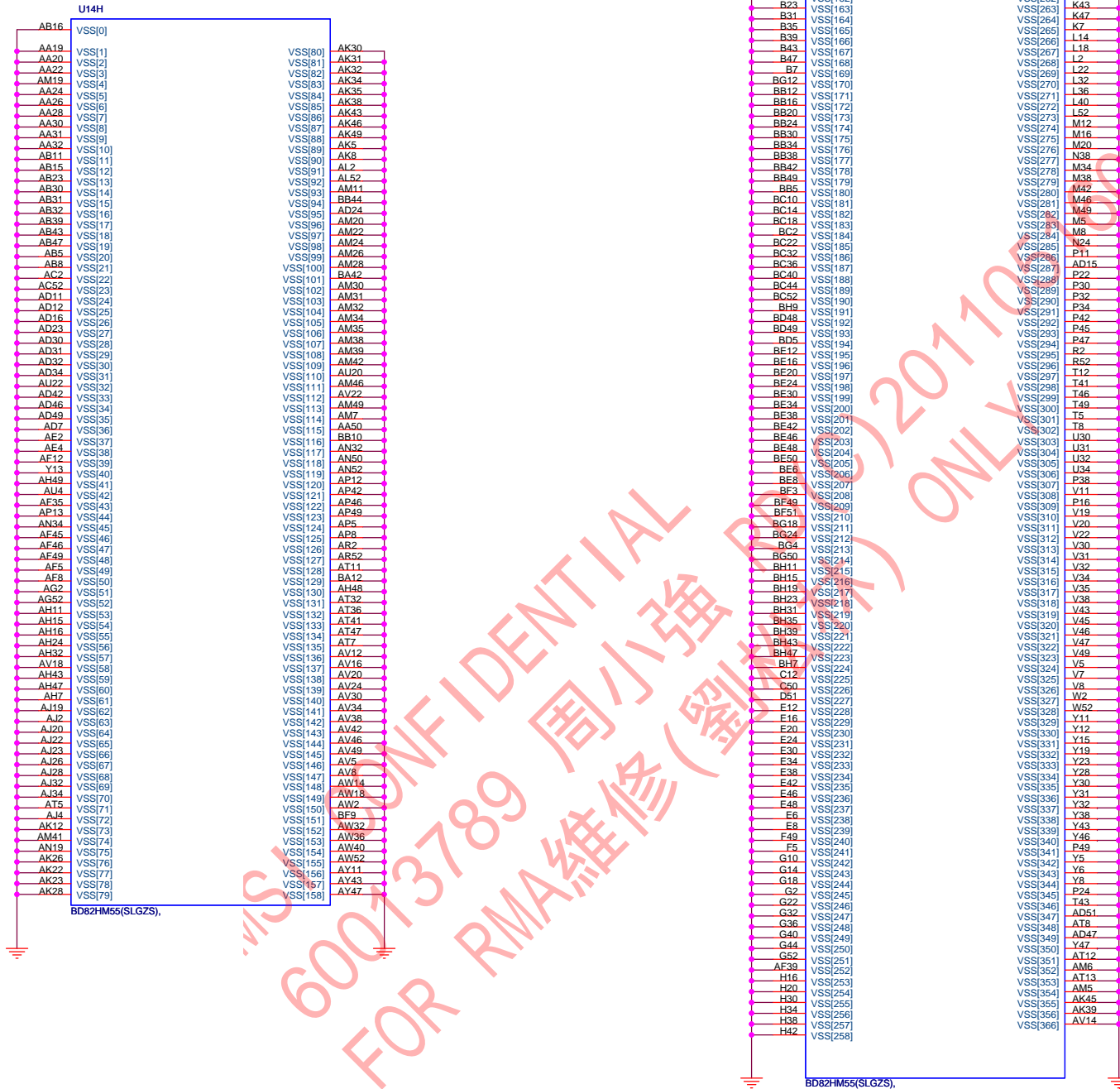


The VCCVRM rail (1.8 V/1.5 V) powers an internal voltage regulator module (VRM) that regulates clean 1.05-V voltage supply for analog rails (VCCAC1k, Vccap11EXP, VCCFDIPLL, and VCCSATAPLL). This solution will allow us to remove the LC filter requirements for those rails, thereby reducing platform BOM cost. VCCVRM is enabled by default via internal pull up to GPIO27, therefore GPIO27 should be left as No Connect. The following diagram shows implementation details on how to enable and disable VccVRM.

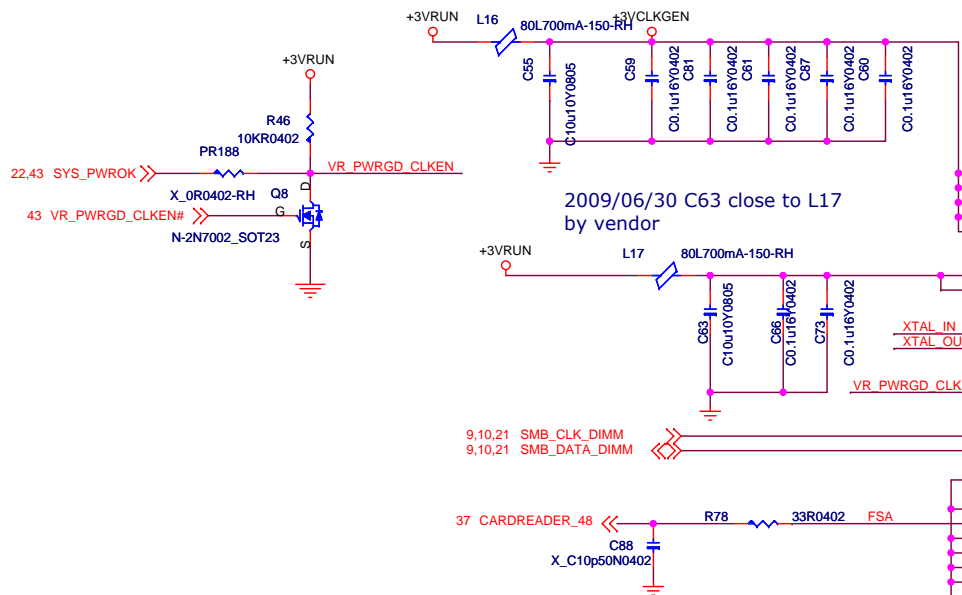


[illegible]

IBEXPEAK - M (GND)



C59 Close to L16 ; C60,C61,C81,C87 Close to power pin



2009/06/30 C63 close to L17 by vendor

9,10,21 SMB_CLK_DIMM
9,10,21 SMB_DATA_DIMM

37 CARDREADER_48

X_C10p50N0402

U13
1 VDD48MHz_3.3
5 VDD_27MHz
17 VDDSRC_3.3
24 VDDCPU_3.3
29 VDDREF_3.3
15 VDDSRC_IO
18 VDDCPU_IO
28 X1
27 X2
25 CLKPWRGD/PD#_3.3
32 SCLK_3.3
31 SDATA_3.3
33 PAD
2 GND48MHz
8 USB48MHz
9 GND27MHz
12 GNDSRC
21 GNDCPU
26 GNDREF

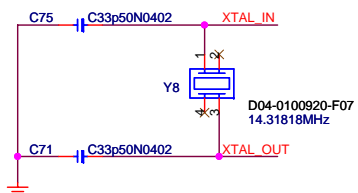
23 CLK_BUF_BCLK_R
22 CLK_BUF_BCLK#_R
20 X
19 X
3 CLK_BUF_DOT96_R
4 CLK_BUF_DOT96#_R
10 CLK_BUF_SATA_R
11 CLK_BUF_SATA#_R
13 CLK_DMI_R
14 CLK_DMI#_R
16 CPU_STOP#
7 CLK_XTAL_27M_S_IN
6 CLK_XTAL_27M_NS_IN
30 CPU_SEL
21 CLK_BUF_BCLK_R
21 CLK_BUF_BCLK#_R
21 CLK_BUF_DOT96_R
21 CLK_BUF_DOT96#_R
21 CLK_BUF_SATA_R
21 CLK_BUF_SATA#_R
21 CLK_BUF_EXP_R
21 CLK_BUF_EXP#_R

2009/06/22
Recommend 4.7KR or 10KR by vendor
For Silego change to 2.2KR

To Park OSC Option

2009/07/08 Reserved for 0A test
R3211 is for Spread clock(Default use)
RB8 is for non-Spread clock

2009/07/08
Y4传049S type(cost down as MS-1122)

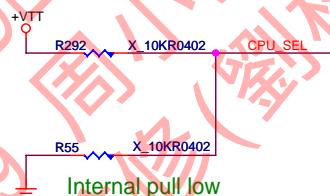


Capacity select

If Cload=20pf C71/C75=33pf

If Cload=32pf C71/C75=56pf

2009/06/30 R292 not stuff

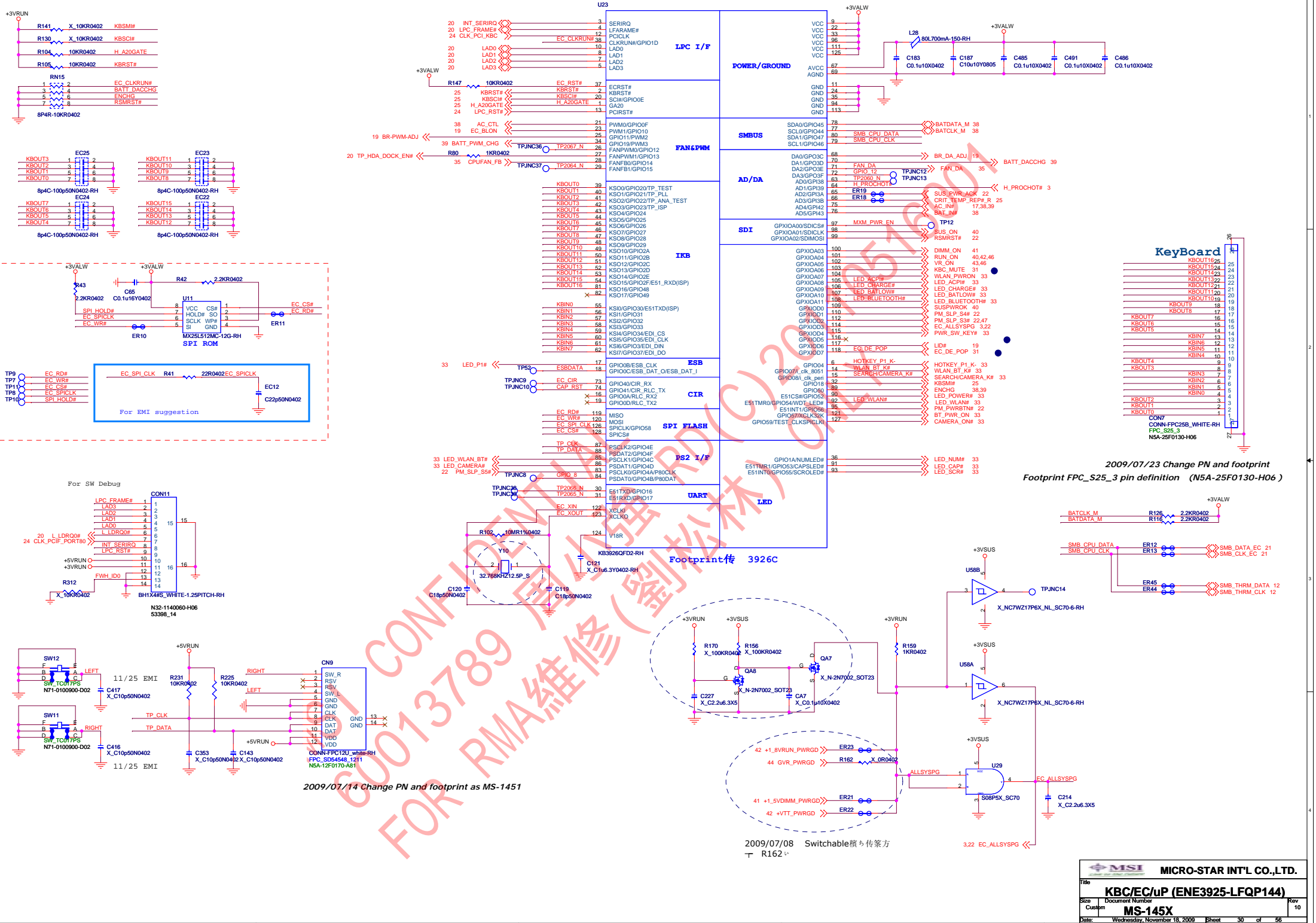


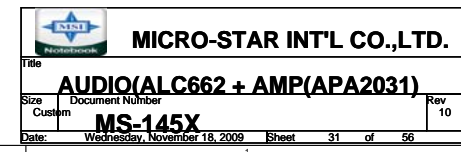
For CPU frequency select (133MHz)

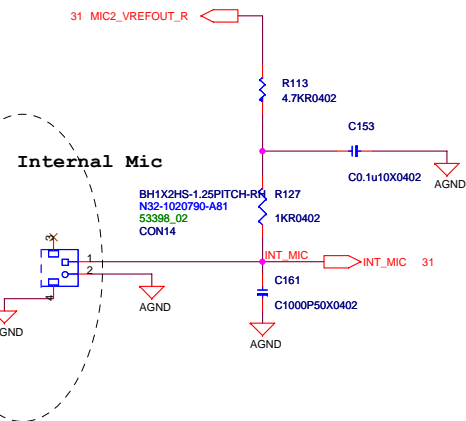
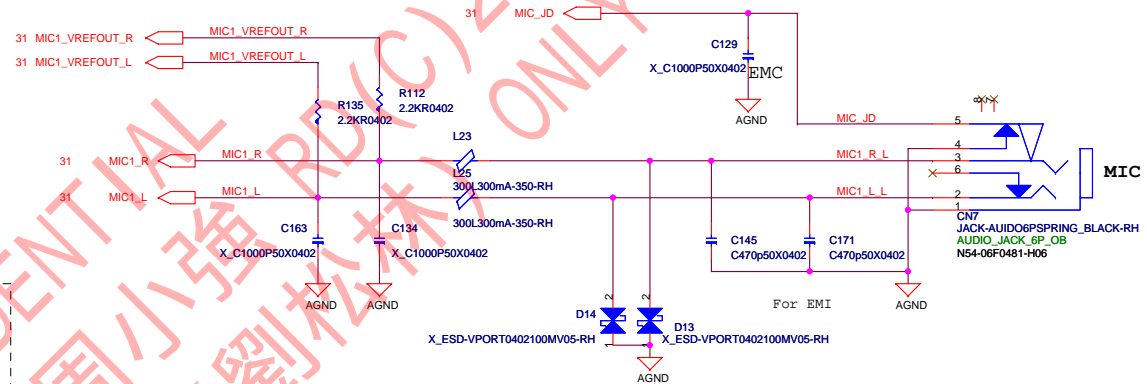
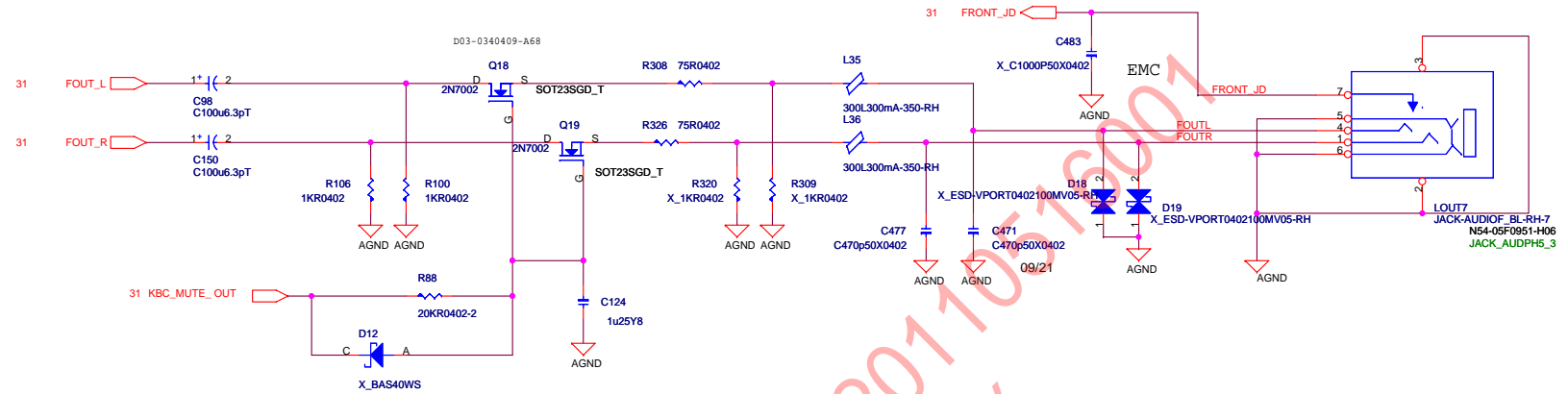
CPU_SEL	CPU0	CPU1
0(Default)	133MHz	133MHz
1(1.05~1.5V)	100MHz	100MHz

Clock GEN. Vendor Table

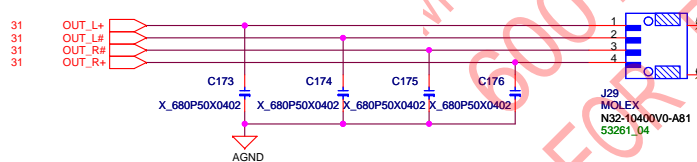
	9LRS3199	SLG8SP587V
VDDIO spec	0.9975~3.465	1.05~3.466
BOM	R39 stuff	R40 stuff





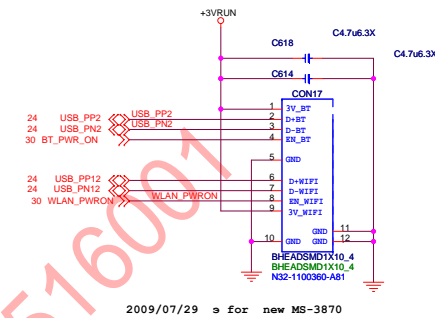
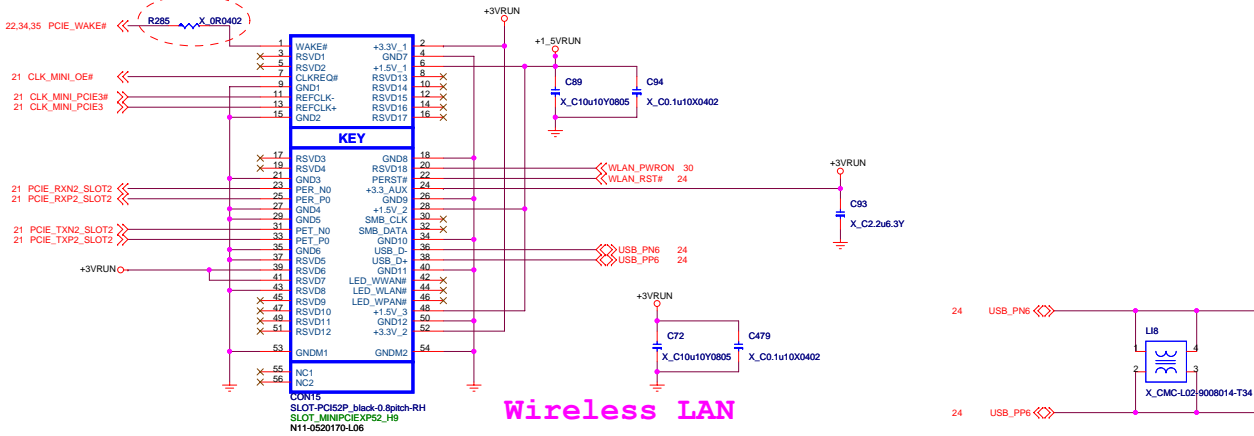


2009/06/29 Modify internal MIC PN to N32-1020790-A81



2009/07/07 0ohm for 變繁Issue

BLUETOOTH



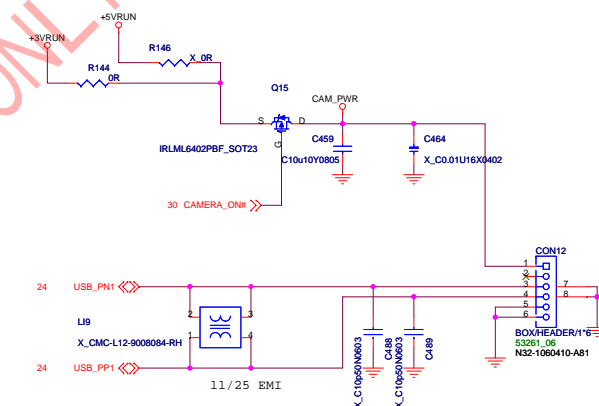
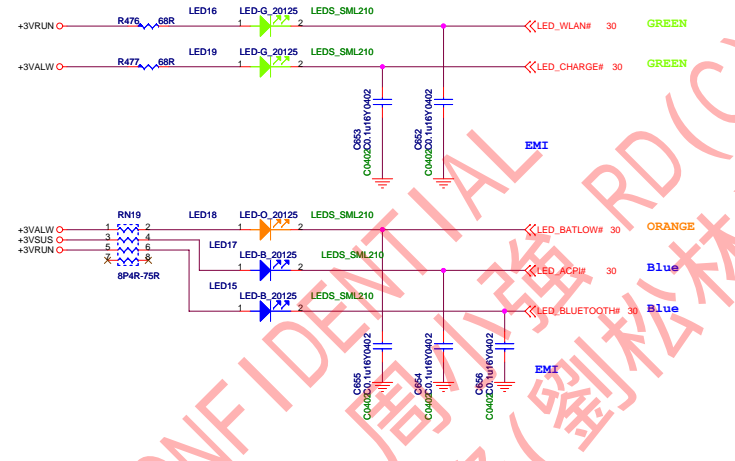
2009/07/29 for new MS-3870

LED light

CAMERA

2009/06/29 Reserved 0 ohm pad by EMI

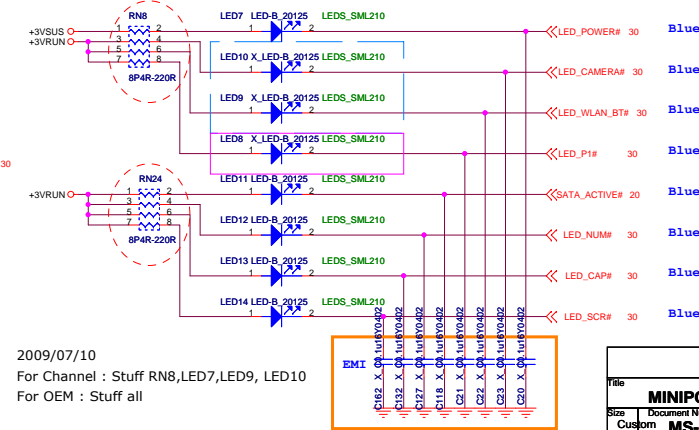
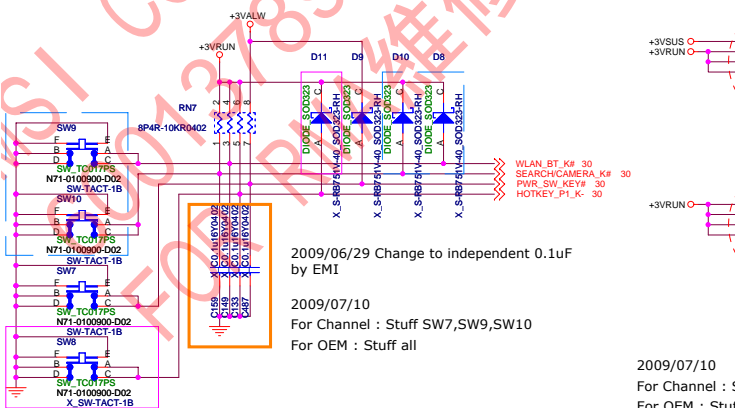
del CN8 0716



	LED7	LED8	LED9	LED10
	SW7	SW8	SW9	SW10
1453	Stuff	Nostuff	Discreate	UMA
1454	Stuff	Nostuff	P1	IE
OEM	Stuff	P1	Wireless	Camera

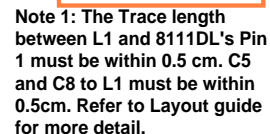
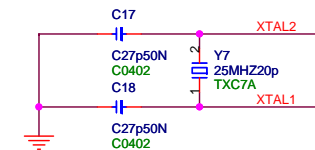
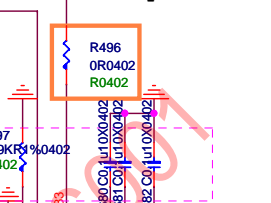
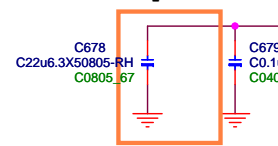
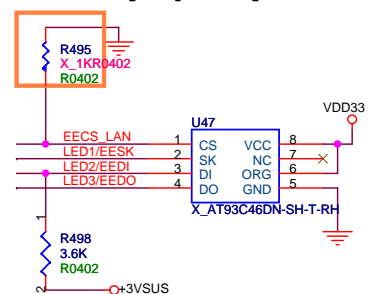
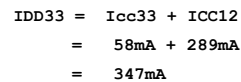
Stuff for CHANNEL

Stuff for OEM



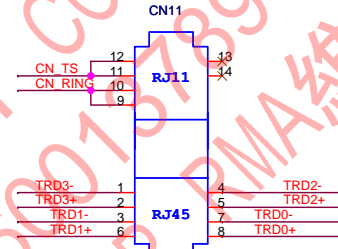
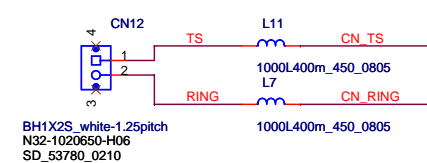
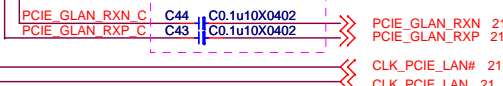
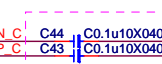
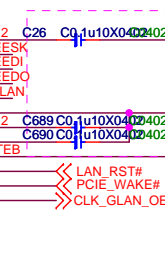
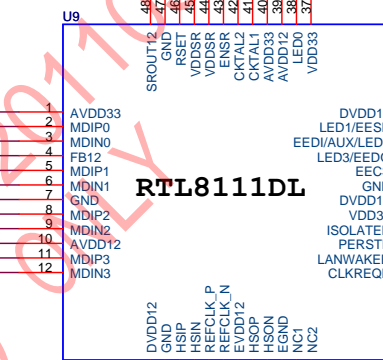
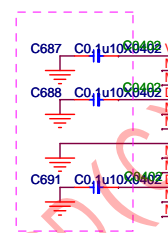
2009/07/10
For Channel : Stuff RN8,LED7,LED9, LED10
For OEM : Stuff all

MSI CORPORATION			
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MINIPCIE,CAMERA,BLUETOOTH,SW		10	
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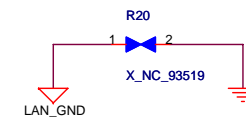
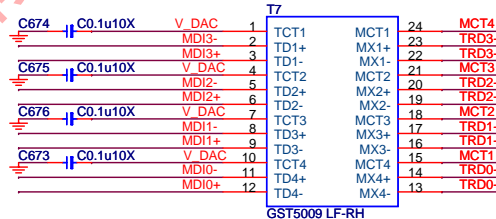


A circuit diagram showing a pull-up resistor R501 (0R0402) connected between VDD33 and CTRL12/VDD.

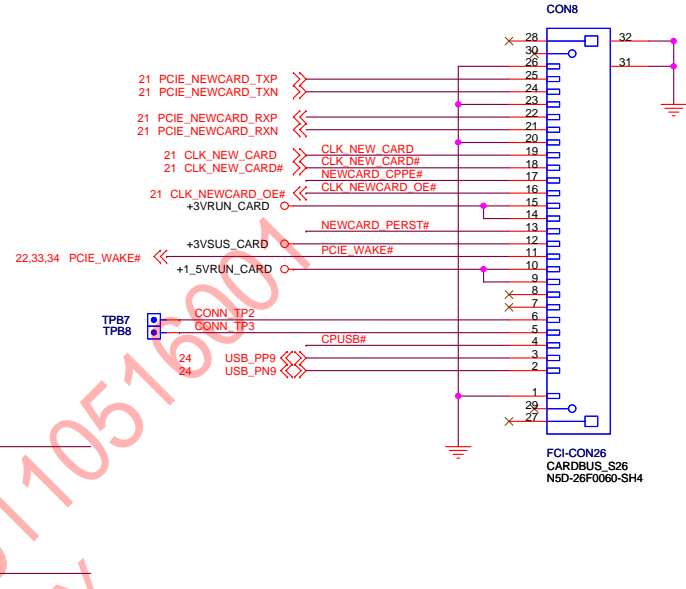
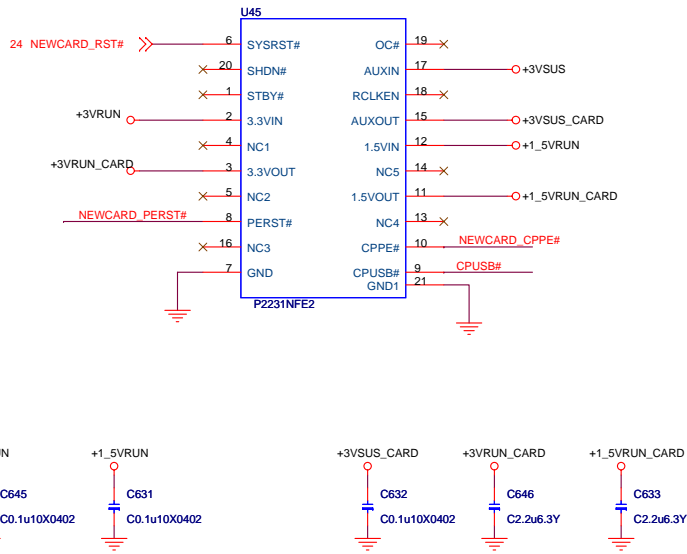
A circuit diagram showing a pull-up resistor R502 (X_0R0402) connected between DVDD12 and CTRL12/VDD.



LTK_RJ4511ROS_RJ4511
N55-12F0110-AF2
RJ45 RJ11 SMT 14P



NEW CARD

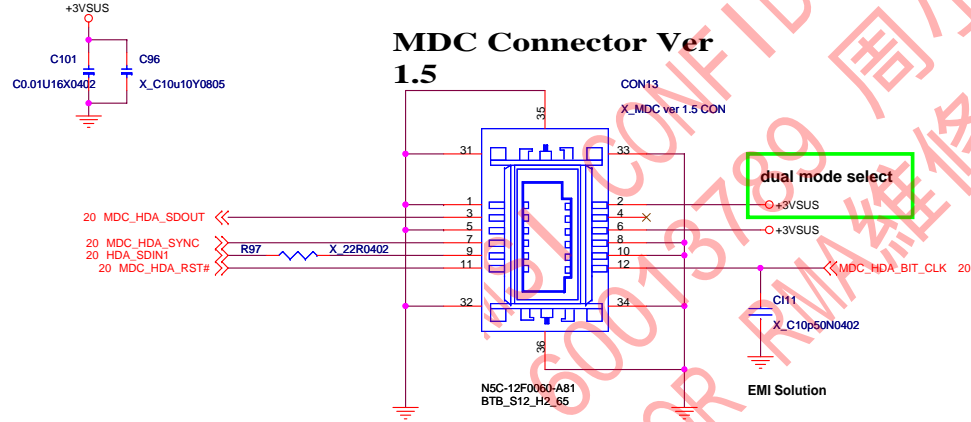


2009/06/26 Reserved by EMI

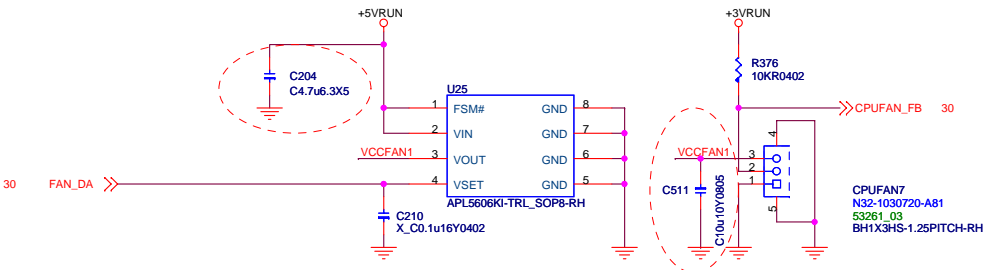
MDC Connector

MDC 1453 NO STUFF; 1454 STUFF!

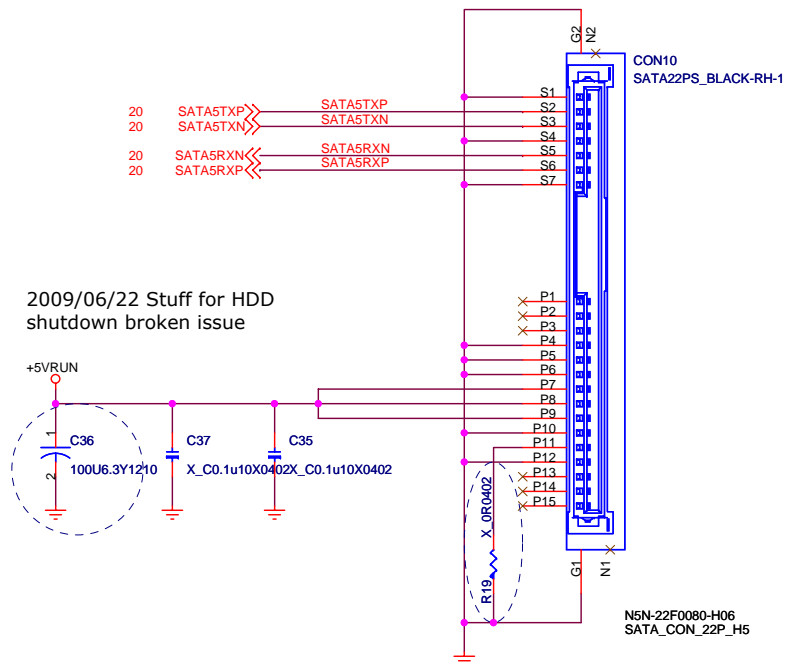
MDC Connector Ver 1.5



CPU FAN

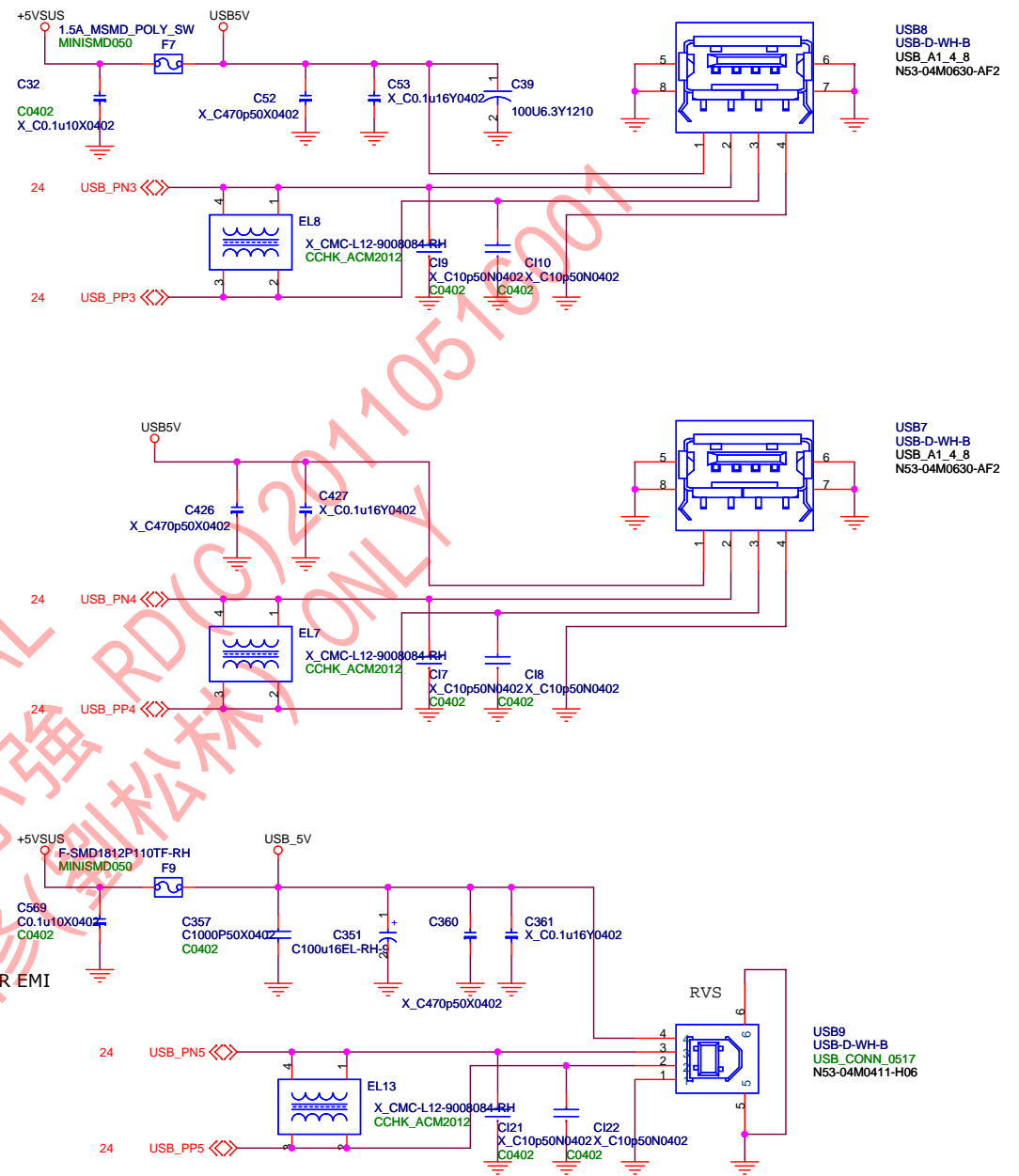
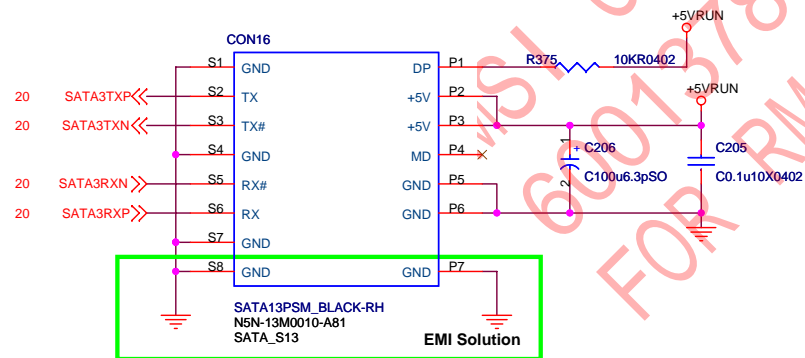


SATA HDD



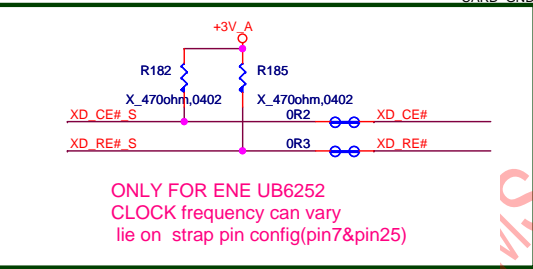
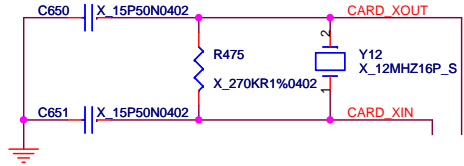
2009/06/22 SATA HDD P11 is Staggered Spinup function

SATA ODD



29 CARDREADER_48 >>> 0R0402 R473 CARD_XIN

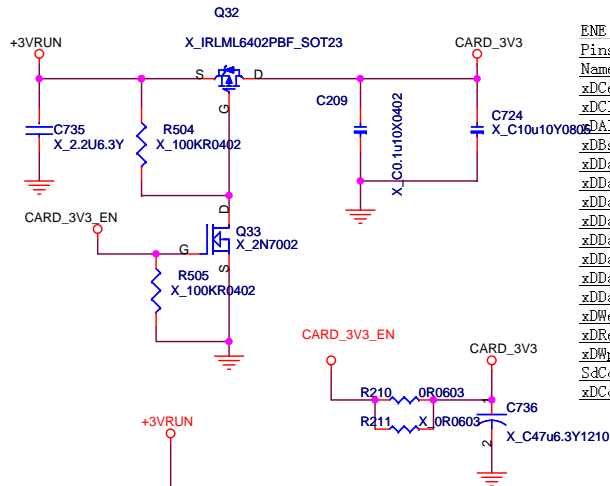
2009/07/01 48MHz from Clock GEN.



ONLY FOR ENE UB6252
CLOCK frequency can vary
lie on strap pin config(pin7&pin25)

Configurations for Clock Source Selection:

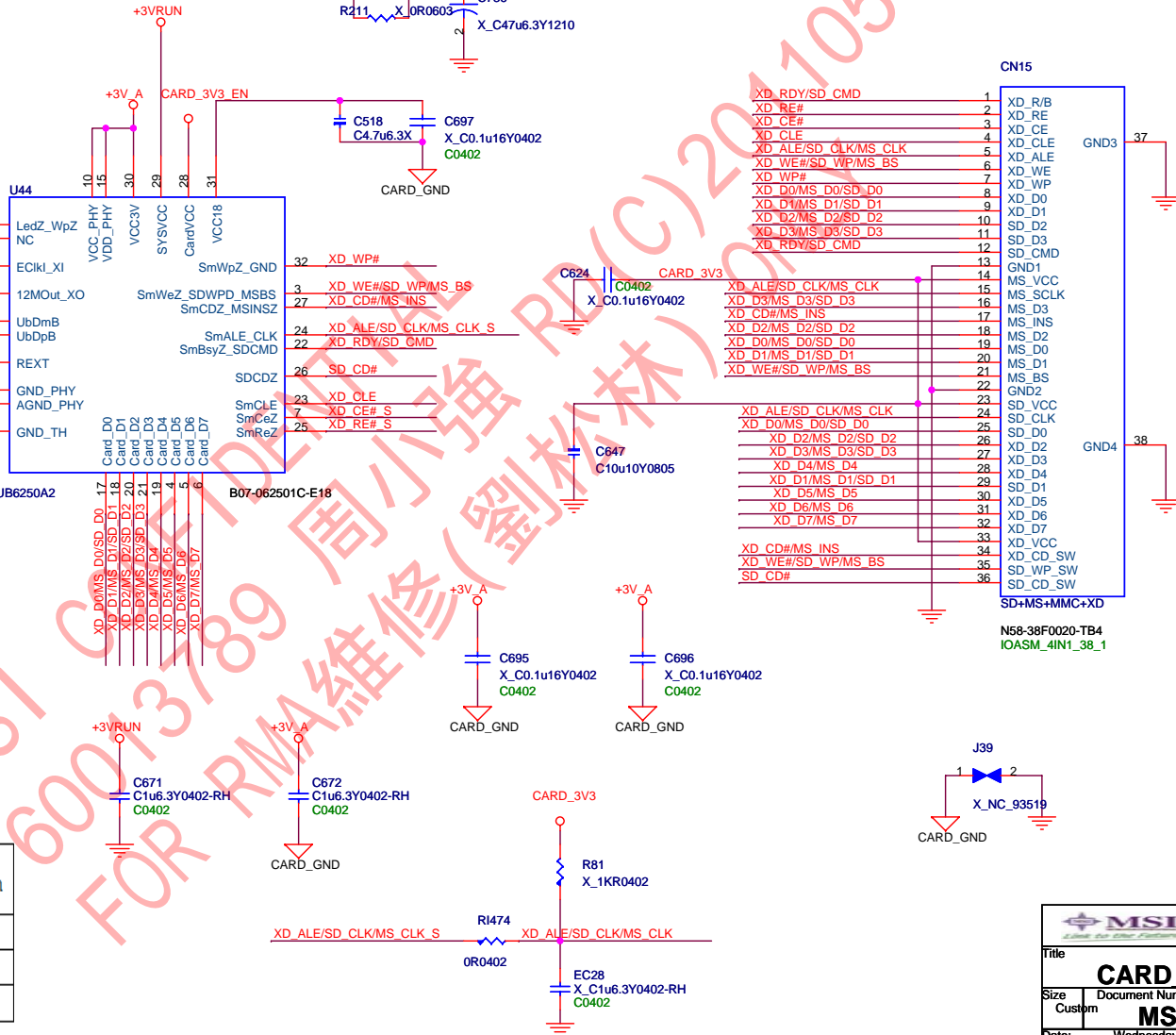
4.7K Pull-high Resistor on		Frequency of external clock source to ECCLK pin
xDrEZ	xDCEZ	
NC	NC	48MHz
NC	O	24MHz
O	NC	12MHz

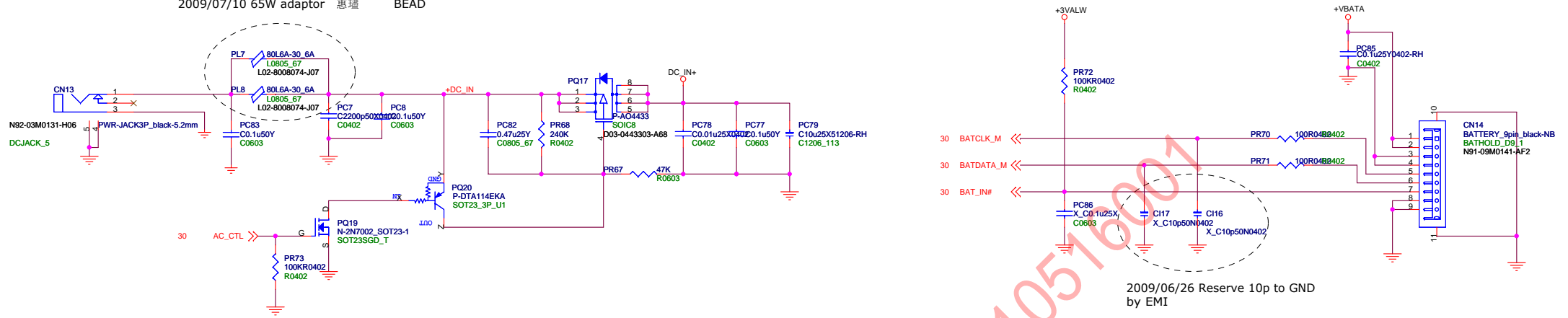


ENE UB6250 USB20 Flash Card Reader Controller

Pins for SD, MMC, MS, and xD memory cards

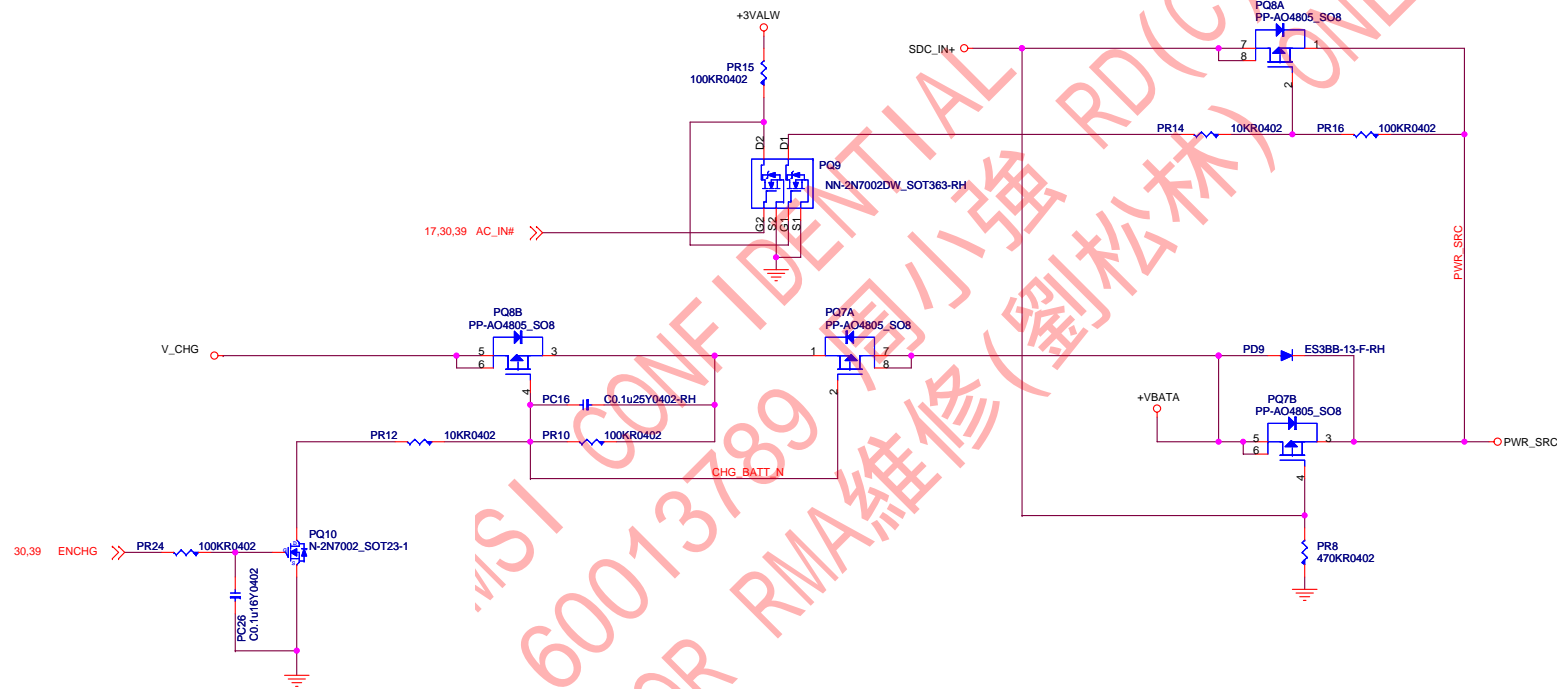
Name	No	I/O	XD	SD	MMC	MS
xDCEZ	7	O	xD card EN			
xDCE	23	O	xD CMD latch EN			
xDAlE	24	O	xD ADDR latch EN	SD clock	MMC clock	MS serial clock
xDByZ	22	B	xD Ready/busy	SD CMD/response	MMC CMD/response	
xDData0	17	B	xD D0	SD D0	MMC D0	MS D0
xDData1	18	B	xD D1	SD D1	MMC D1	MS D1
xDData2	20	B	xD D2	SD D2	MMC D2	MS D2
xDData3	21	B	xD D3	SD D3	MMC D3	MS D3
xDData4	19	B	xD D4		MMC D4	MS D4
xDData5	4	B	xD D5		MMC D5	MS D5
xDData6	5	B	xD D6		MMC D6	MS D6
xDData7	6	B	xD D7		MMC D7	MS D7
xDWeZ	3	B	xD W EN	SD WP		MS Busy
xDReZ	25	O	xD R EN			
xDWpZ	32	O	xD WP			
SDCDZ	26	I		SD CD	MMC CD	
xDcZ	27	I	xD CD			MS CD





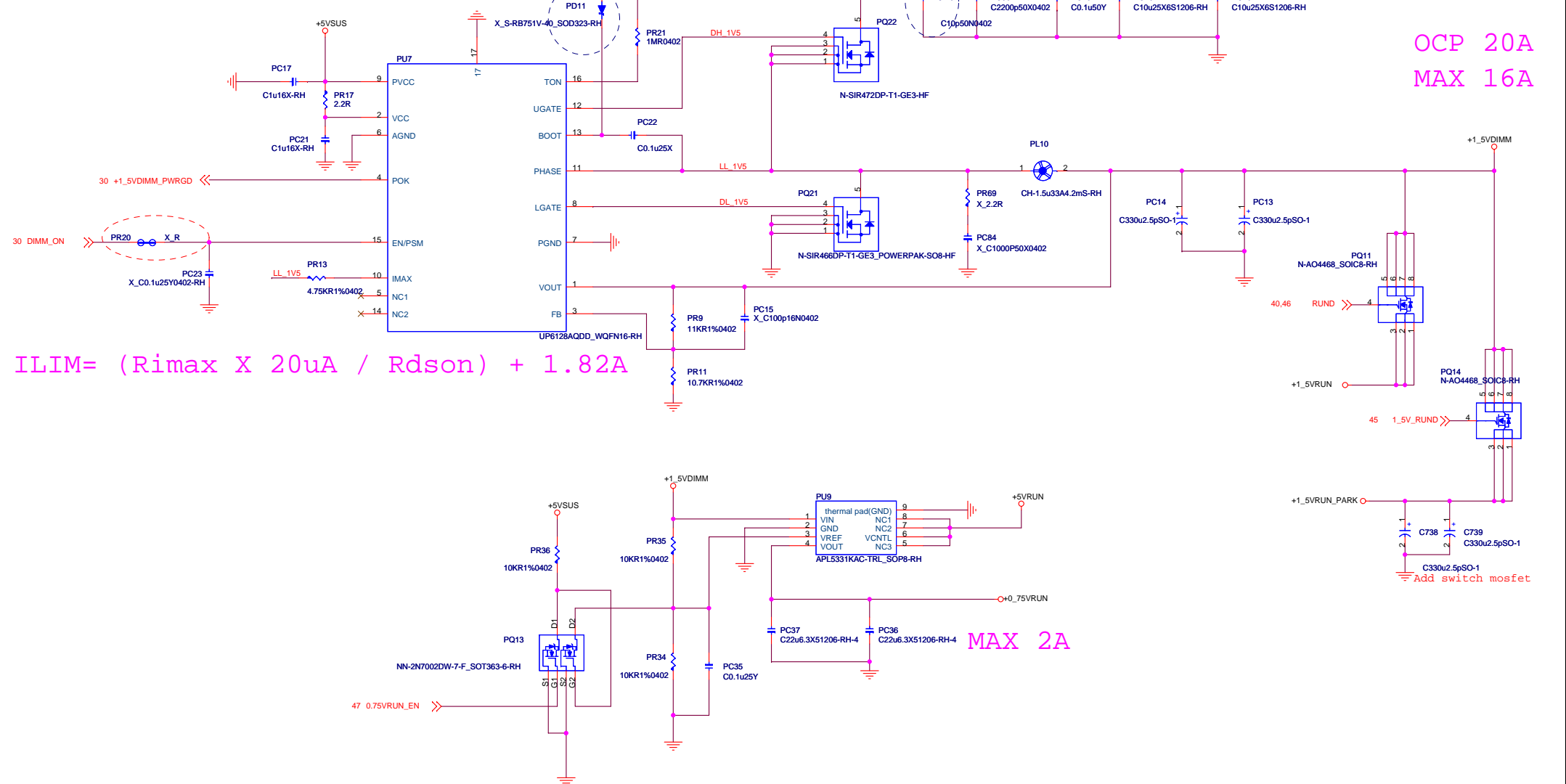
JBAT1 Pin Definition

- 1: VBATA+
- 2: VBATA+
- 3: NC
- 4: NC
- 5: SMBCLK
- 6: SMBDATA
- 7: BAT_IN#
- 8: GND
- 9: GND



2009/07/10 轟と 瞬ノ

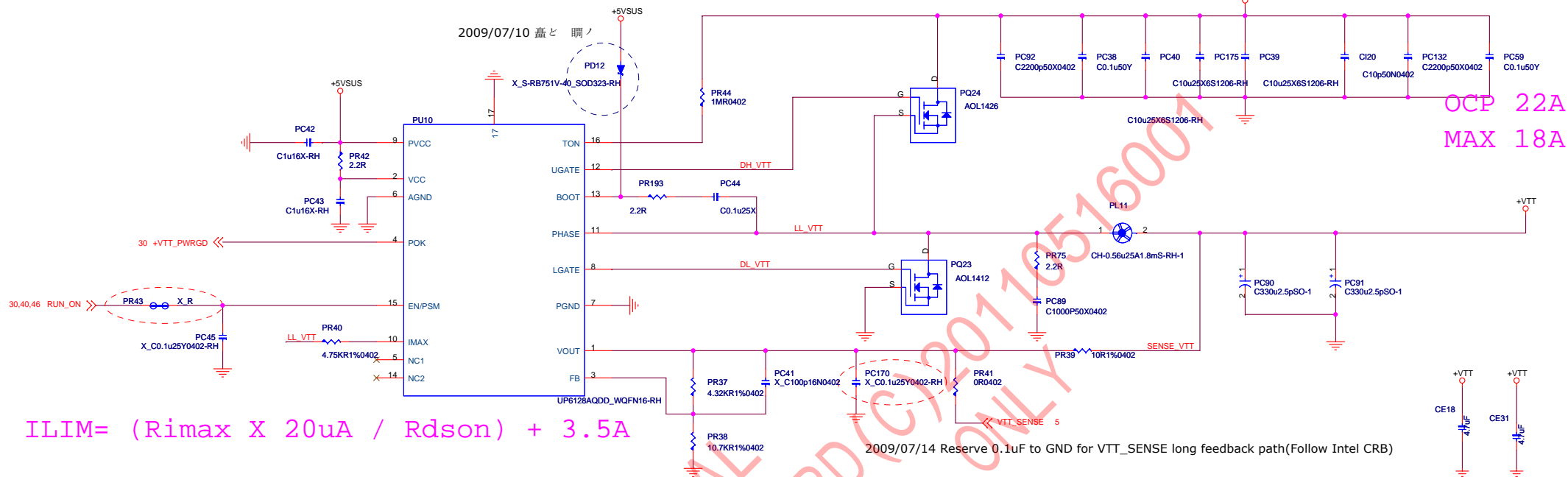
2009/06/26 Reserve 10p to GND
by EMI (Close to PQ21)



$$ILIM = (R_{imax} \times 20\mu A / R_{dson}) + 1.82A$$

2009/07/10 蠡と 瞬ノ

2009/06/26 Reserve 10p to GND
by EMI (Close to PQ23)

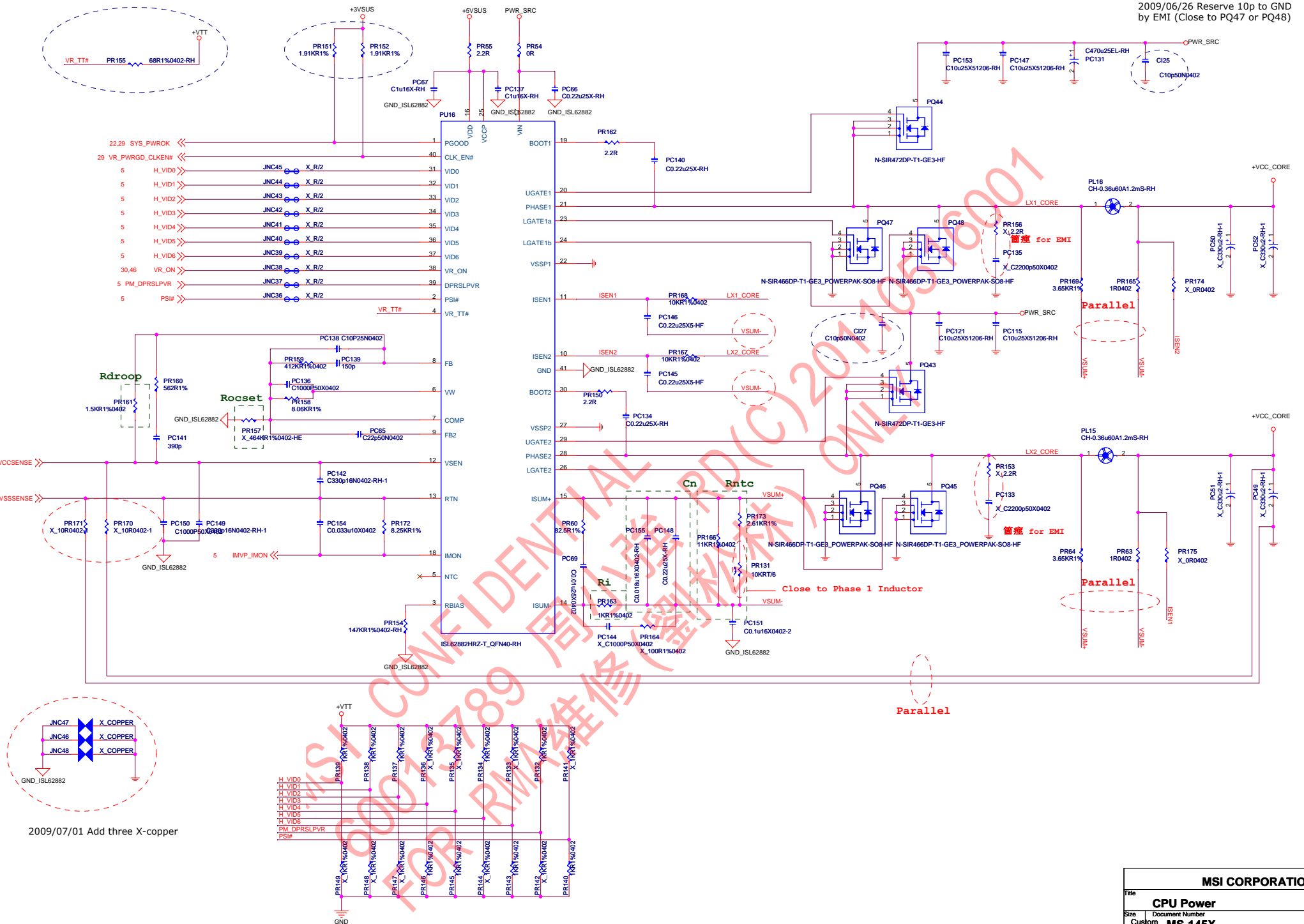


Modify net name

Maximum 2A

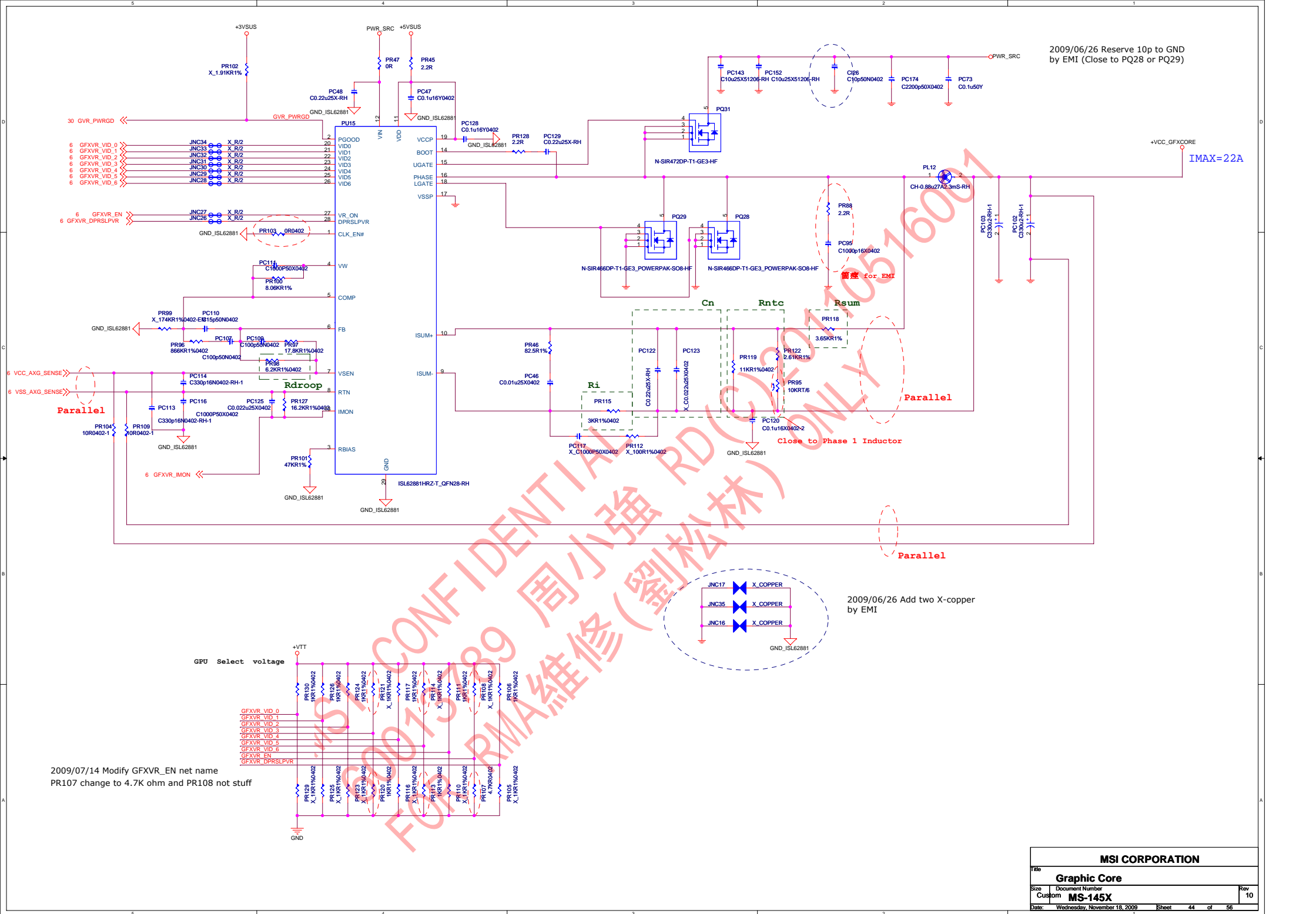
Add MLCC cap

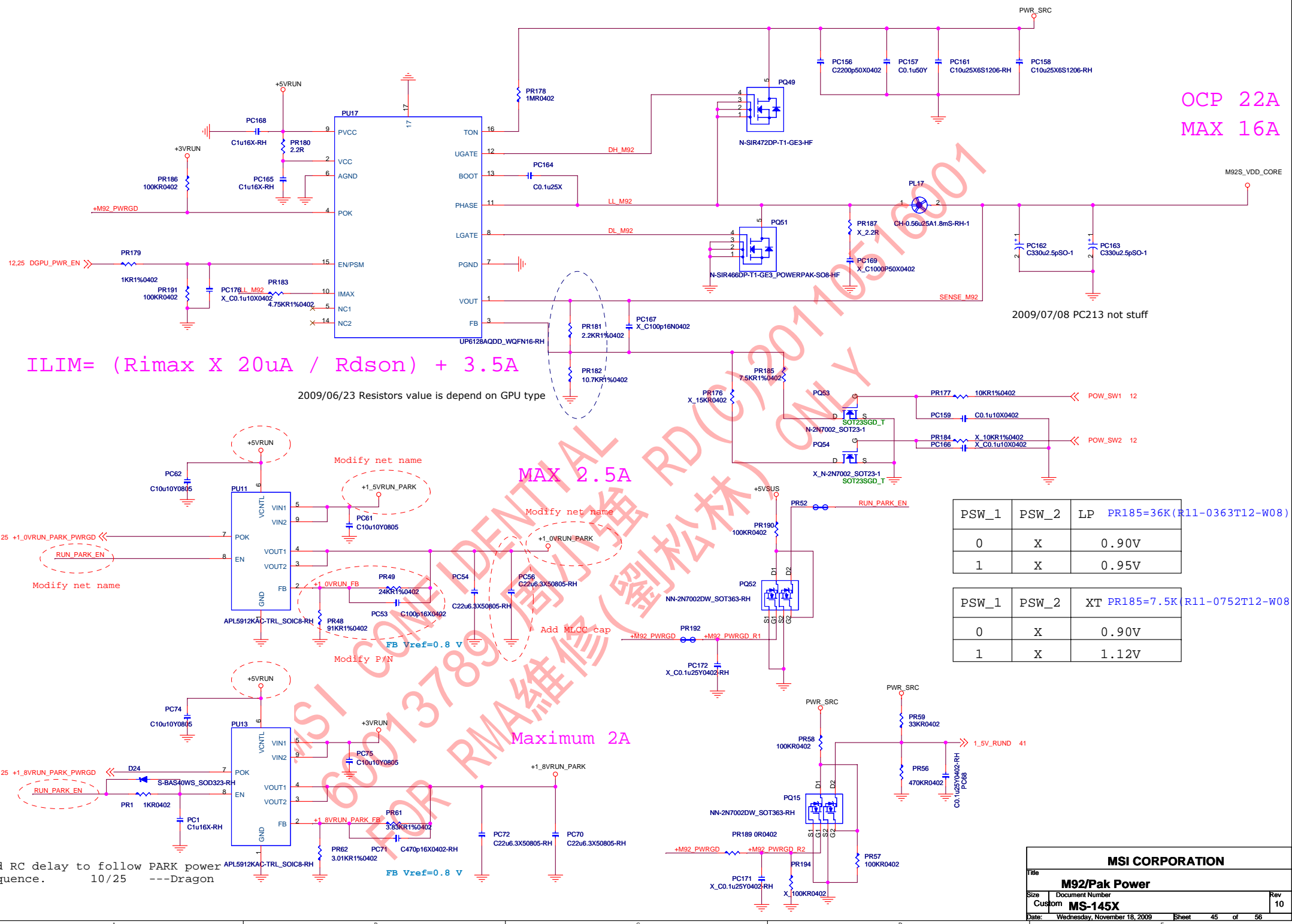
2009/06/26 Reserve 10p to GND
by EMI (Close to PQ47 or PQ48)



2009/07/01 Add three X-copper

MSI CORPORATION			
Title			
CPU Power			
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$$I_{LIM} = (R_{imax} \times 20\mu A / R_{dson}) + 3.5A$$

2009/06/23 Resistors value is depend on GPU type

OCF 22A
MAX 16A

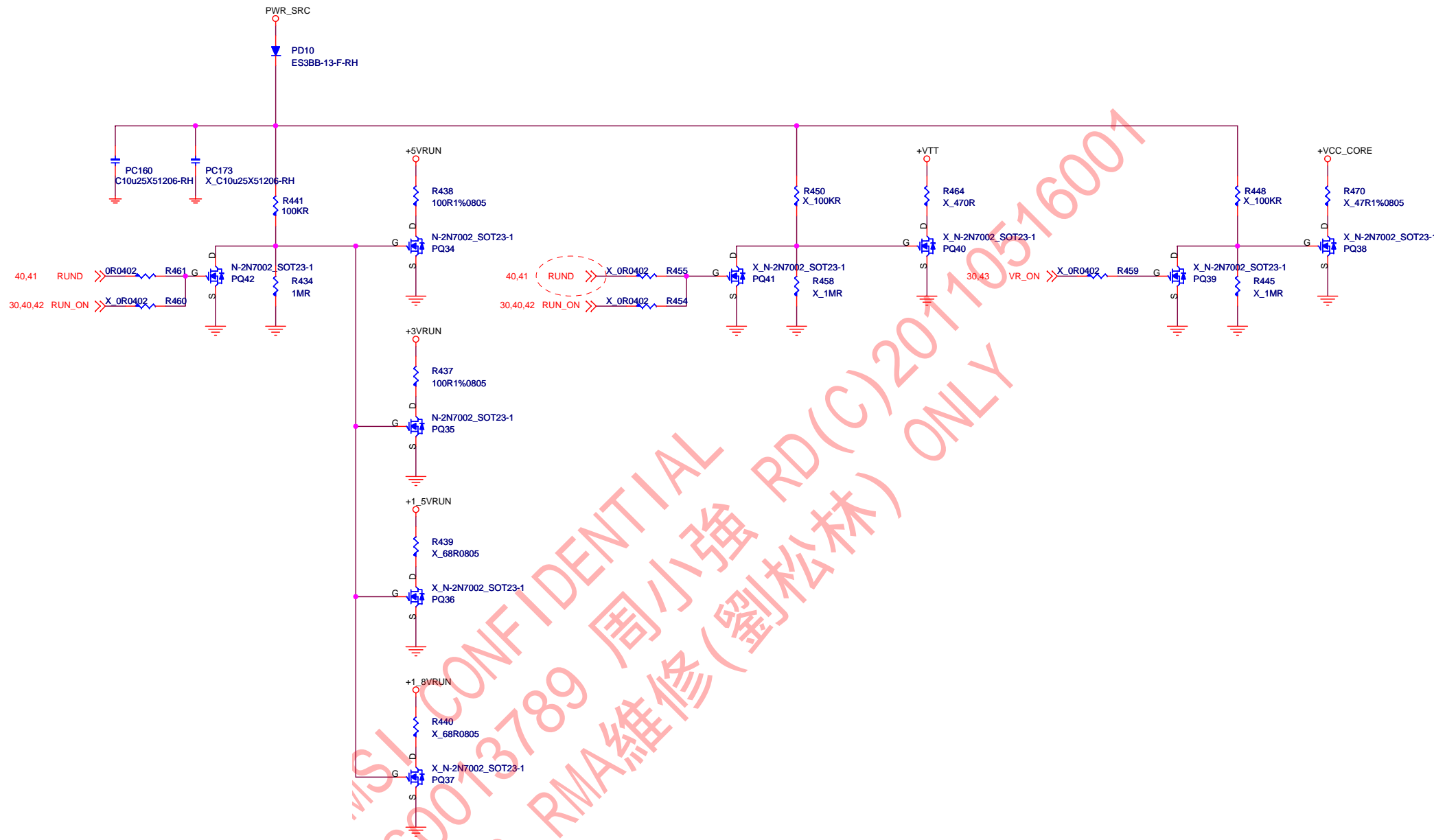
MAX 2.5A

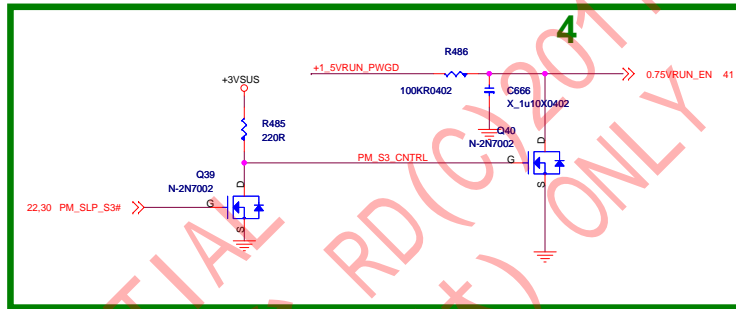
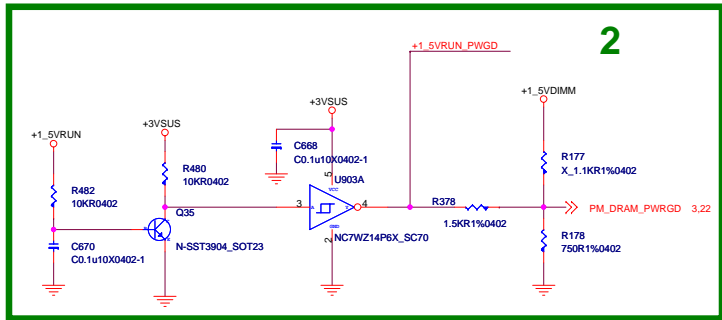
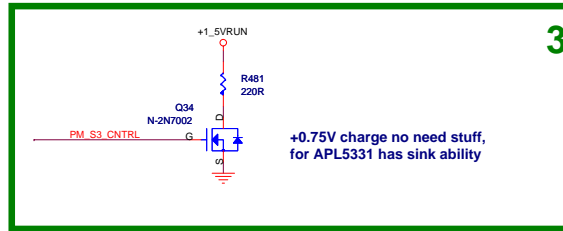
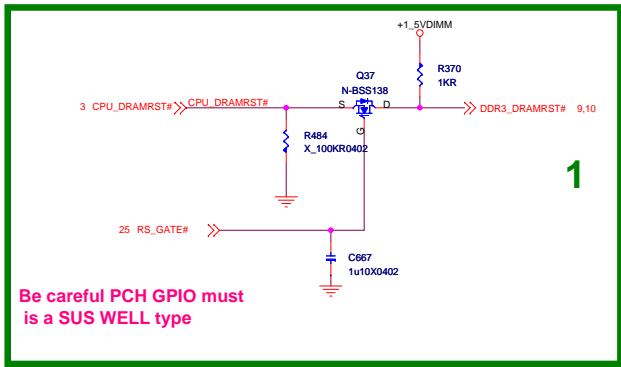
Maximum 2A

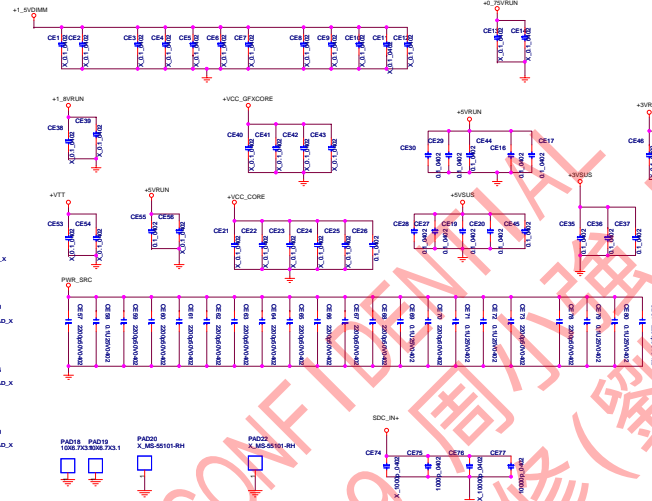
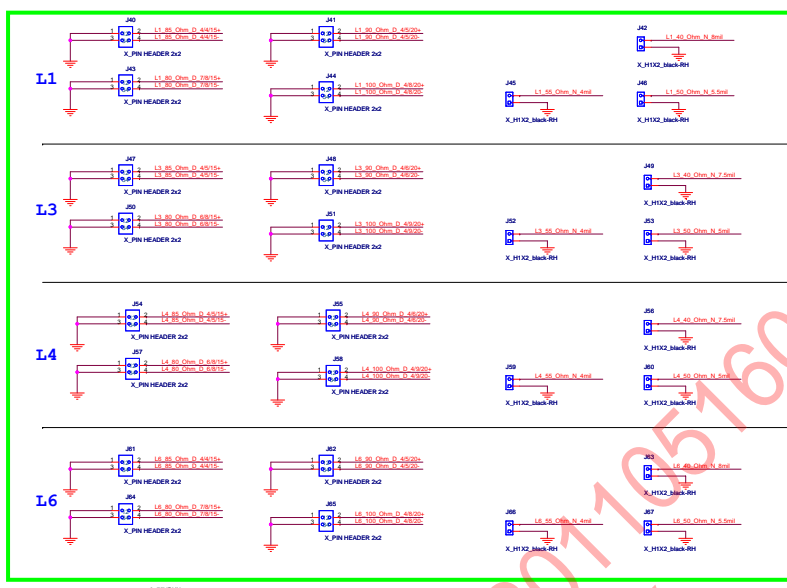
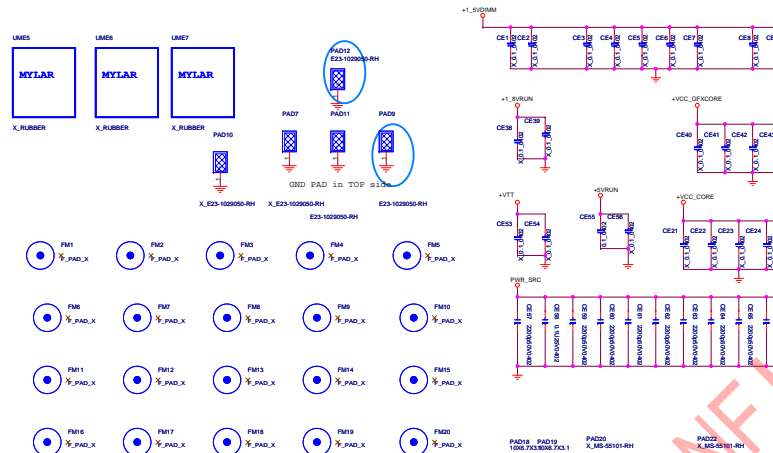
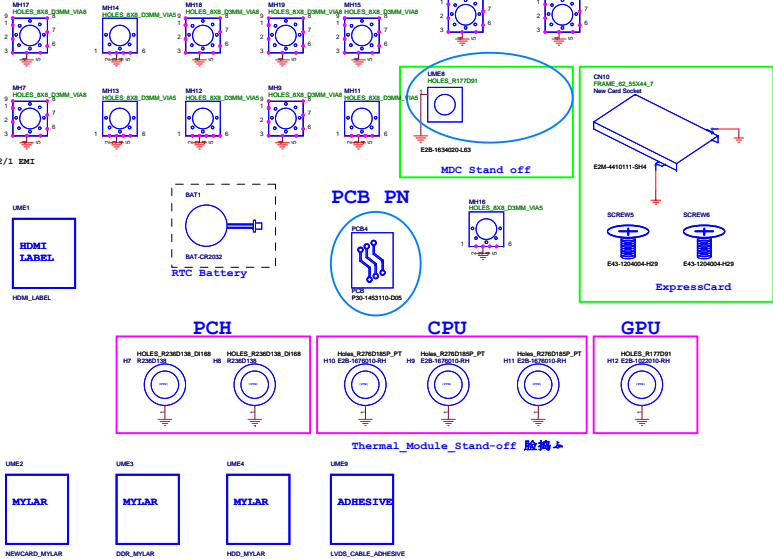
PSW_1	PSW_2	LP	PR185=36K(R11-0363T12-W08)
0	X		0.90V
1	X		0.95V

PSW_1	PSW_2	XT	PR185=7.5K(R11-0752T12-W08)
0	X		0.90V
1	X		1.12V

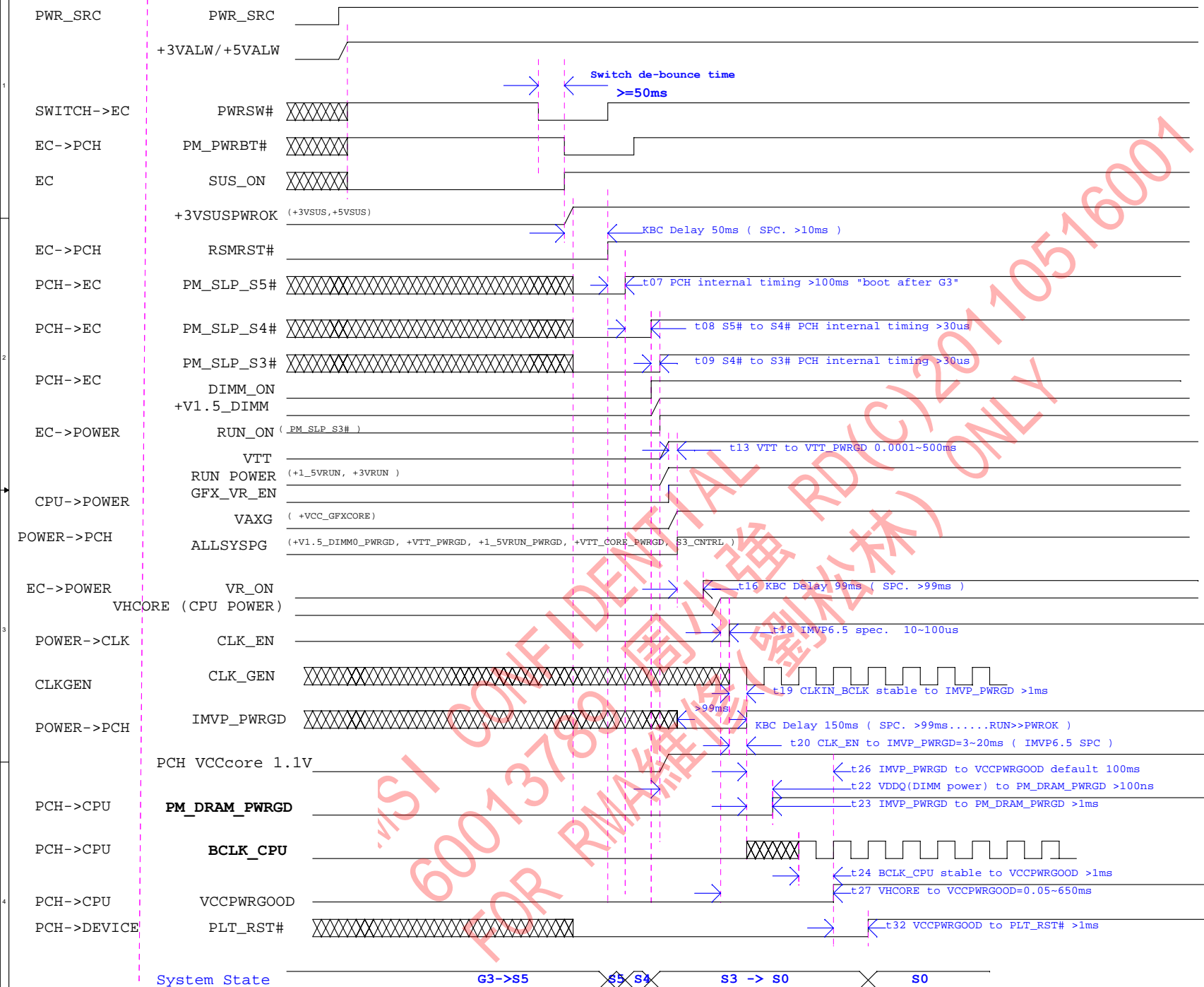
Add RC delay to follow PARK power sequence.
10/25 ---Dragon



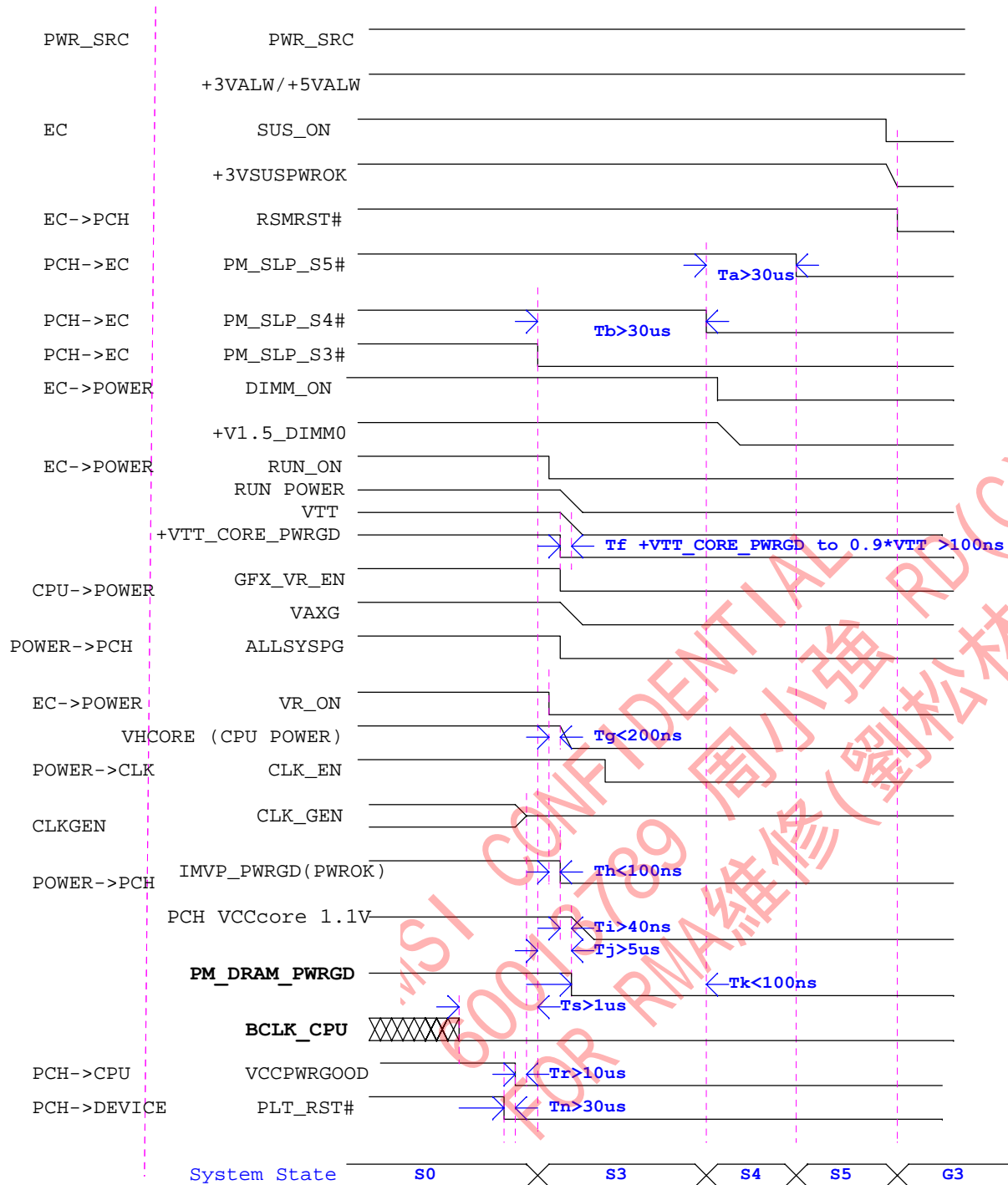


[illegible]

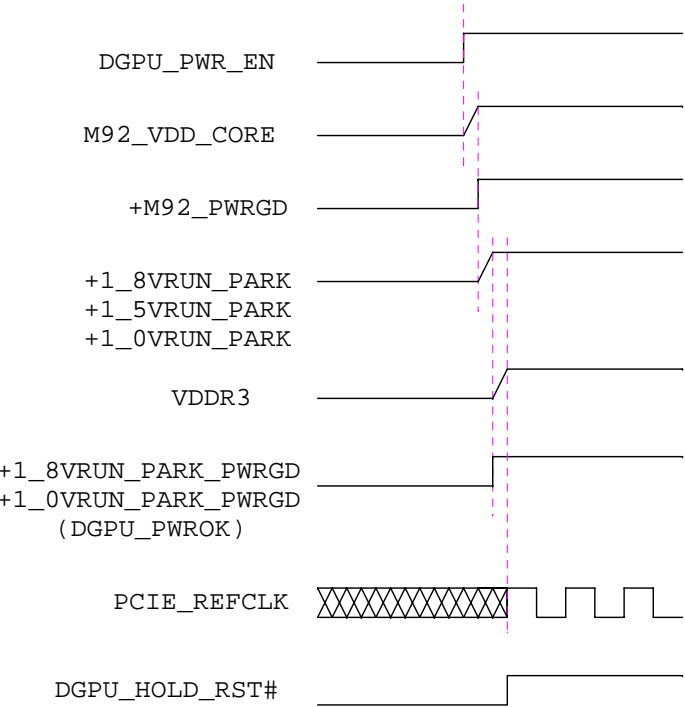
Calpella System Power on Sequence DC mode



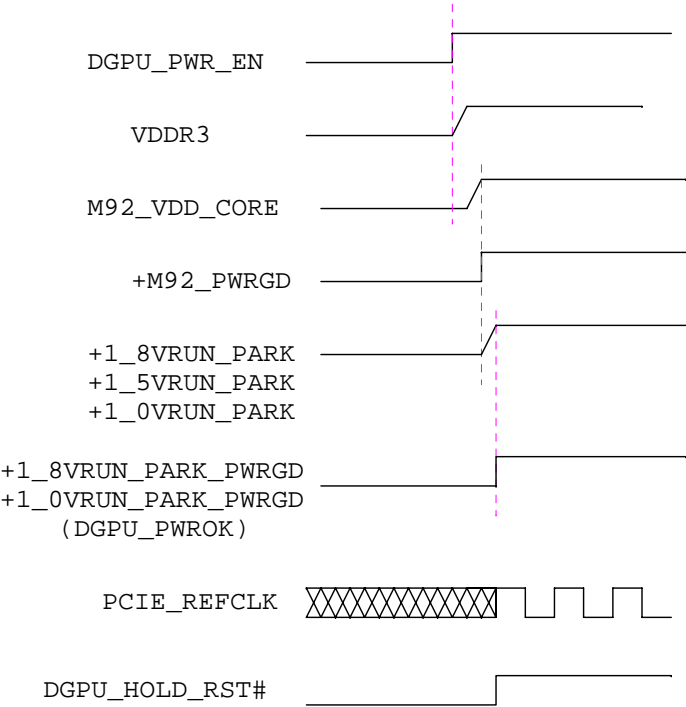
Power down Sequence DC mode S0 to G3



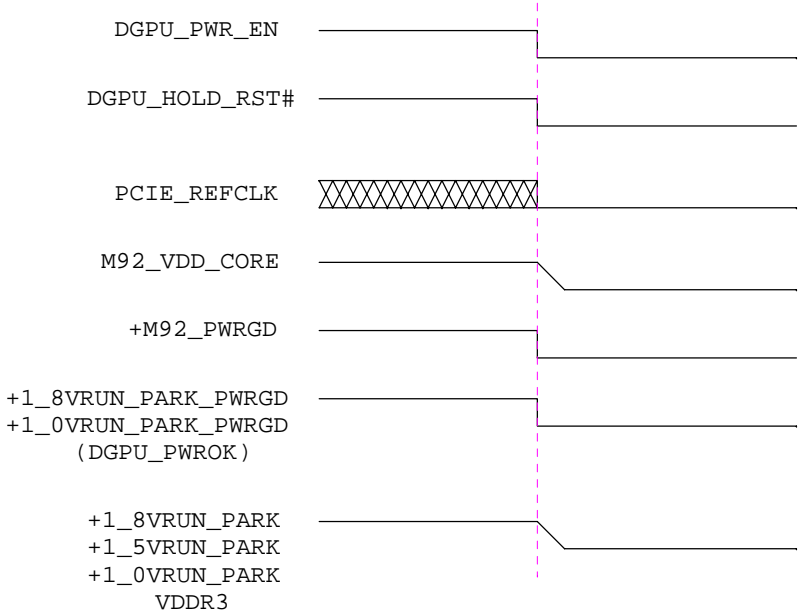
M92 Power on Sequence



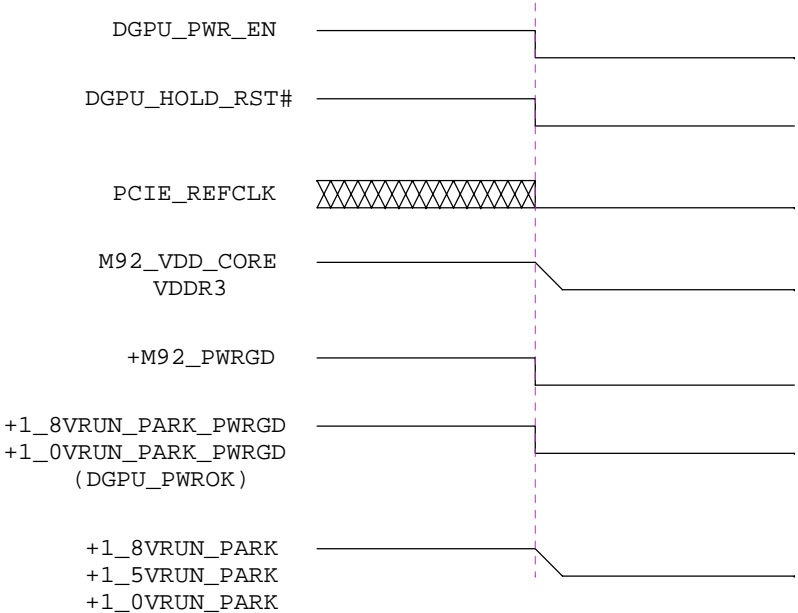
PARK Power on Sequence



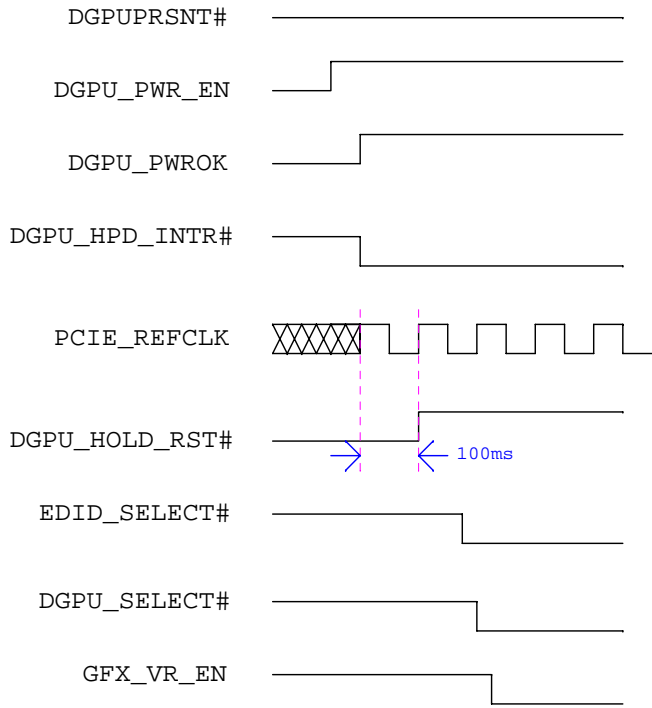
M92 Power down Sequence



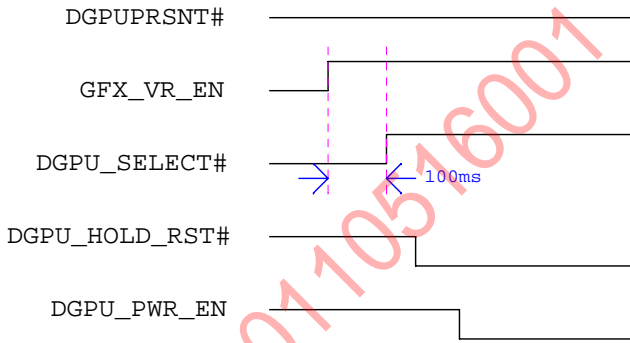
PARK Power down Sequence

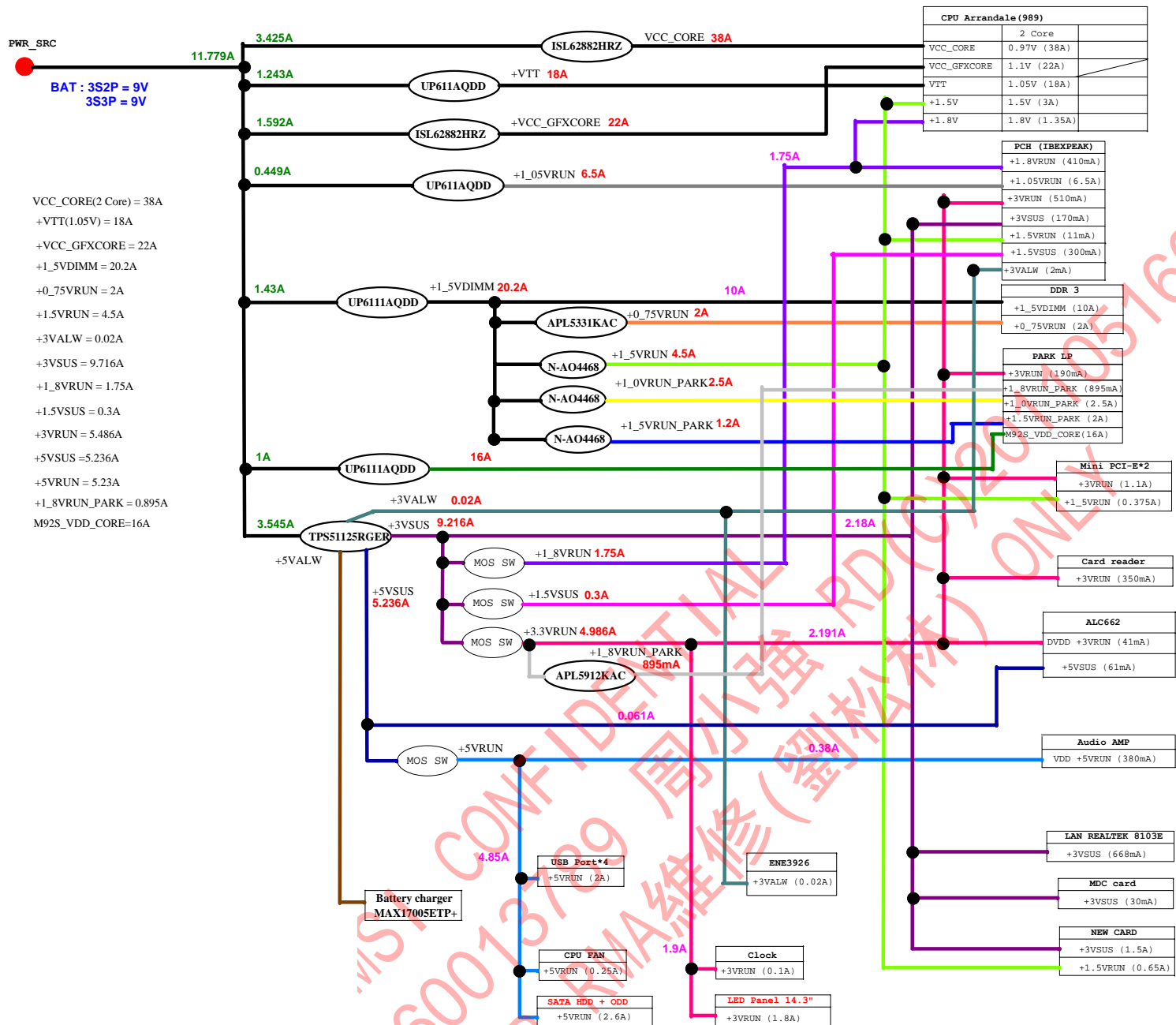


Switchable DGPU Power on Sequence
Discrete Mode



Switchable DGPU Power off Sequence
UMA Mode



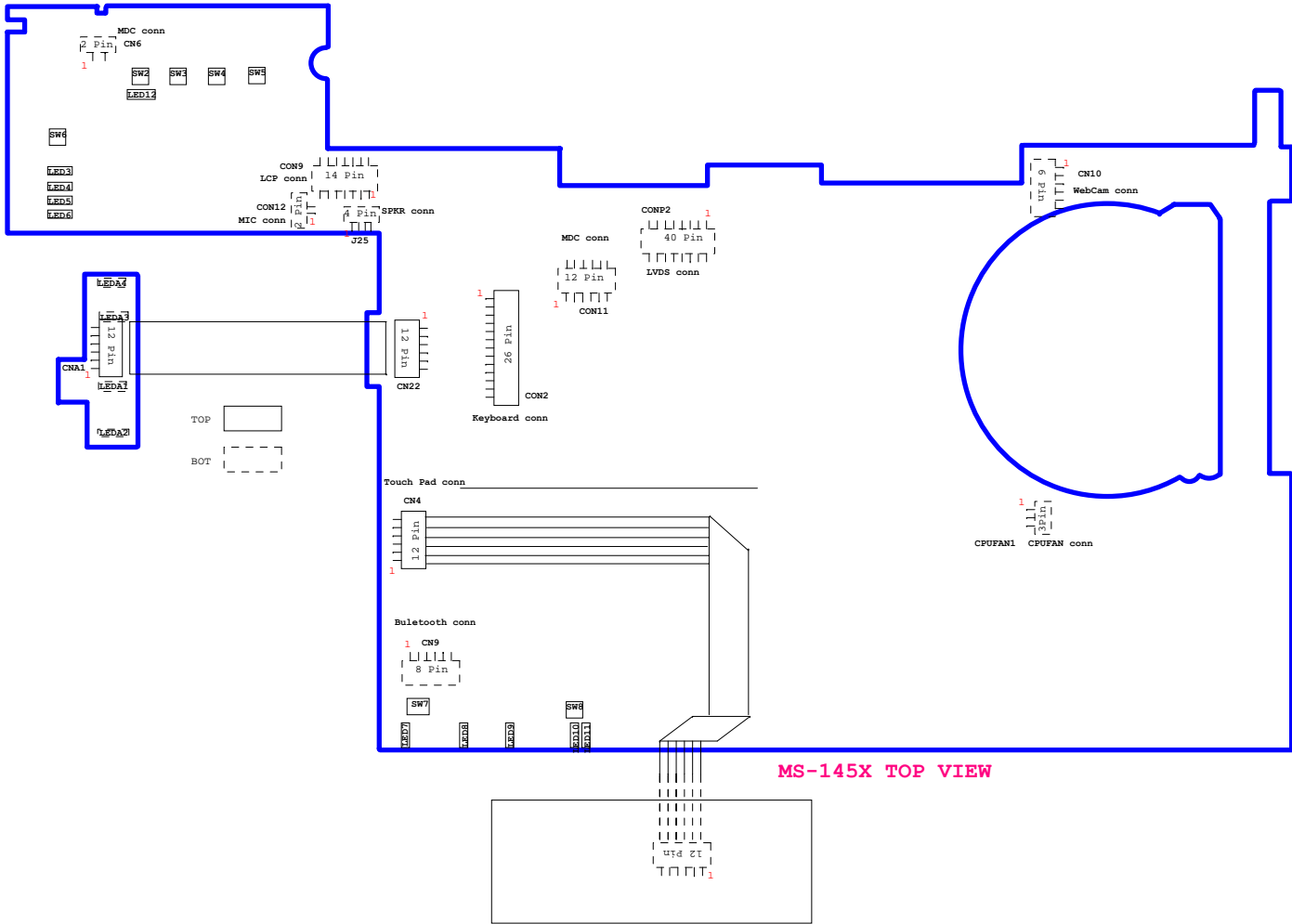


MS-145X	
SW2	Power_button(FOR OEM)
SW3	HotKeyF1_button(FOR OEM)
SW4	WLAN/BT_button(FOR OEM)
SW5	Search/Webcam_button (FOR OEM)
SW6	Power_button(FOR Channel)
SW7	Right_button
SW8	Left_button

MS-145X	
LED3	HDD_LED (FOR OEM)
LED4	NUM_LED (FOR OEM)
LED5	CAP_LED (FOR OEM)
LED6	SCR_LED (FOR OEM)
LED7	BT_LED
LED8	WLAN_LED
LED9	ACPI_LED
LED10	CHARGE_LED
LED11	BATTERY_LOW_LED
LED12	POWER_LED

MS-145XA	
LEDA1	NUM_LED (FOR OEM)
LEDA2	HDD_LED (FOR OEM)
LEDA3	CAP_LED (FOR OEM)
LEDA4	SCR_LED (FOR OEM)

MS-145X : Main Board
MS-145XA : LED board



MS-145X TOP VIEW

2009/06/25 [Page33] Add LED and switch function for OEM reserved
[Page30] Delete KBOUT16,KBOUT17 for MS-1451 keyboard matrix
[Page41/42] Modify APL5912 VCNTL to +5VSUS
[Page43/44] Modify some RC footprint and value

2009/06/26 Modify circuit to Switchable
[Page19] Add LVDS common choke by EMI
[Page12] Reserve RGB 10p to GND
[Page38] Reserve BAT CLK and DATA 10p to GND
[Page39] Reserve 10p SDC_IN+ to GND and close to PQ57
Add two X-Copper
[Page40] Reserve 10p +5VSUS to GND and close to PQ60
Reserve 2.2R+2200p
[Page41] Reserve 10p PWR_SRC to GND and close to PQ68
[Page42] Reserve 10p PWR_SRC to GND and close to PQ72
[Page43] Reserve 10p PWR_SRC to GND and close to PQ75 or PQ76
Reserve 10p PWR_SRC to GND and close to PQ78 or PQ79
[Page43] Reserve 10p PWR_SRC to GND and close to PQ81 or PQ82
Add two X-Copper

2009/06/29 [Page35] Modify CPU FAN.Add C121 and C304 by datasheet.Add one more RC for FAN speed calculation(as MS-1122)
Modify PARK circuit
Modify PCH PN to OB1-1675001 for Mobile IntelR 5 Series Chipset Full Feature
Modify Audio jack PN to N54-05F0951-H06
Modify internal MIC PN to N32-1020790-A81
Modify power sequence map

2009/07/01 [Page3] R234,R412单0A龟喷挡獠 / 彡 殄 簿埃
BPM#[0~7] remove
BCLK 獠痠from PCH,簿埃from CLOCK GEN.

[Page5] Short bead

[Page6] Short bead

[Page7] VSS_NCTF1~7 remove

[Page8] 獠痠CFG 代獠,尤縮簿埃

[Page9] SA0_DIM0のSA1_DIM0 0 ohm癸
簿埃330uF, CPU のswitching power狼 T

[Page10] SA0_DIM1 0 ohm癸
簿埃330uF, CPU のswitching power狼 T

[Page12] 干 HPD紲隔

[Page16] MDA0~MDA7 swap

[Page18] CRTのLVDS 簡痠箒 (for MS-1454)A 虫聳 0 ohm
EDID switch 箒方pin 0.1uF
R3238,R3239 10K ohm
簿埃BR-AD-ADJ,BR-PWM-ADJ 嘿 PWM-ADJ,HDMI DDC 嘿 HDM_SDAのHDM_SCL

[Page19] 貳獨LC 0.1uH+10pF
穢穢LVDS DDC pull high,backlight adj簡痠net PWM-ADJ

[Page25] DGPUPRSNT# 0pull down

[Page30] 0+1_8VRUN_PARK_PWRGDの+1_0VRUN_PARK_PWRGD挡 DGPU_PWROK

[Page34] C47,C49 0.1uF

[Page43] Add three X-copper

10 VER

[Page21] Add GPU leakage circuit

[Page12] Reserve TEST_EN / JTAG_TMS pull high R for AMD recommend
Reserve GPIO26_TCK circuit for AMD recommend
Reserve JTAG_TRSTB pull low R for AMD recommend

[Page18] Change D23 P/N to D01-BAS4000-W01
for HDMI fail

[Page36] Change F9 P/N to D08-0100110-P16
for USB HDD shut down issue

[Page36] Change C351 P/N to C98-1011650-P01
for USB HDD shut down issue

[Page31] Stuff R134 for internal speaker POP noise.

[Page45] Add RC delay to follow PARK power sequence.

[Page12] GPIO26_TCK pull down through 10k R229.